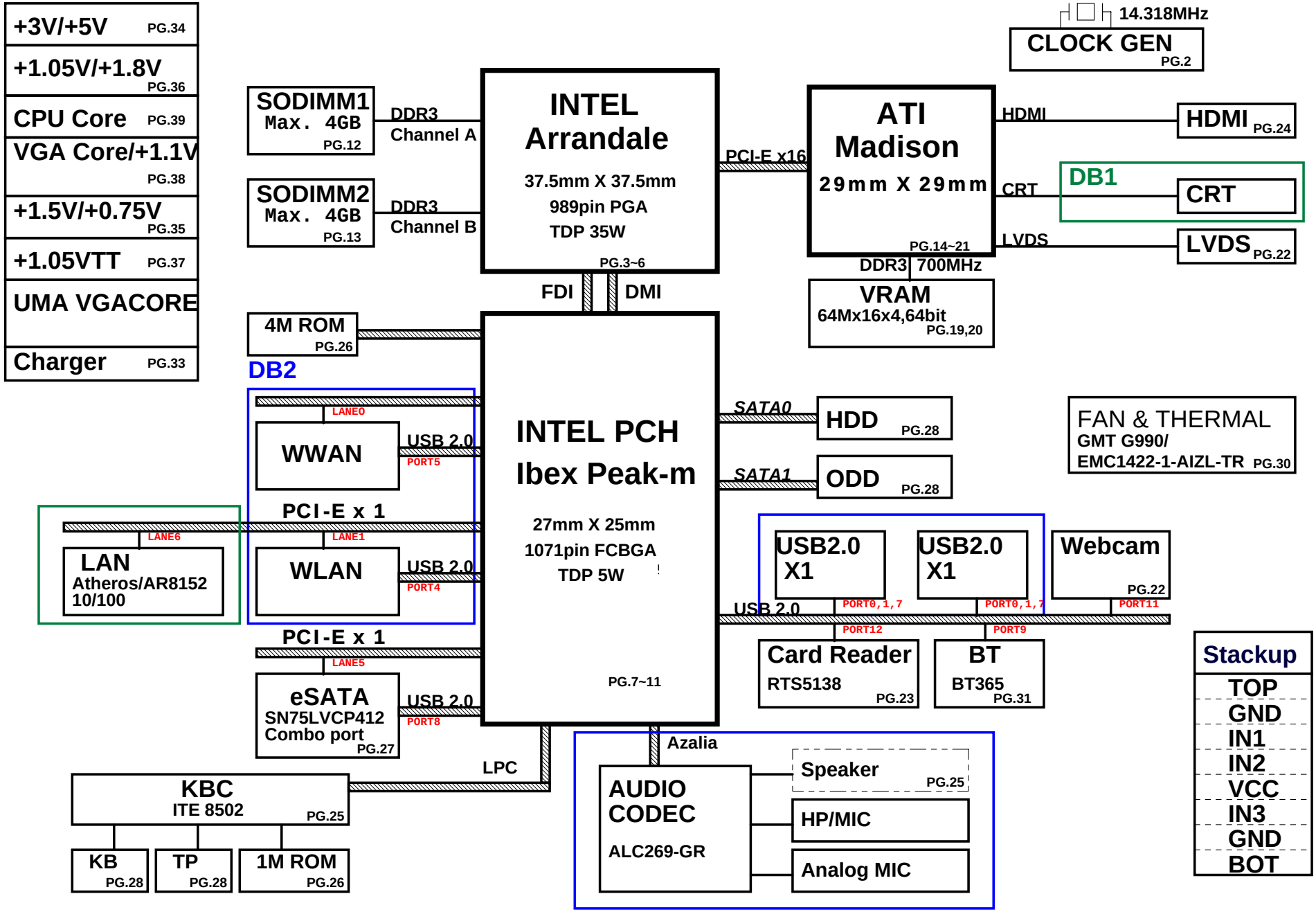
UM8B DIS SYSTEM DIAGRAM



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PROJECT : UM8B DIS

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

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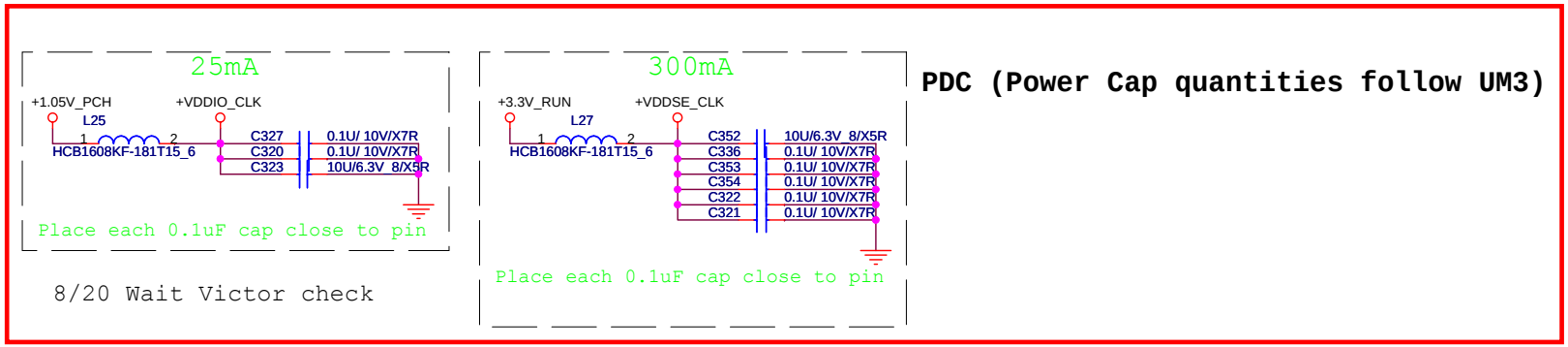
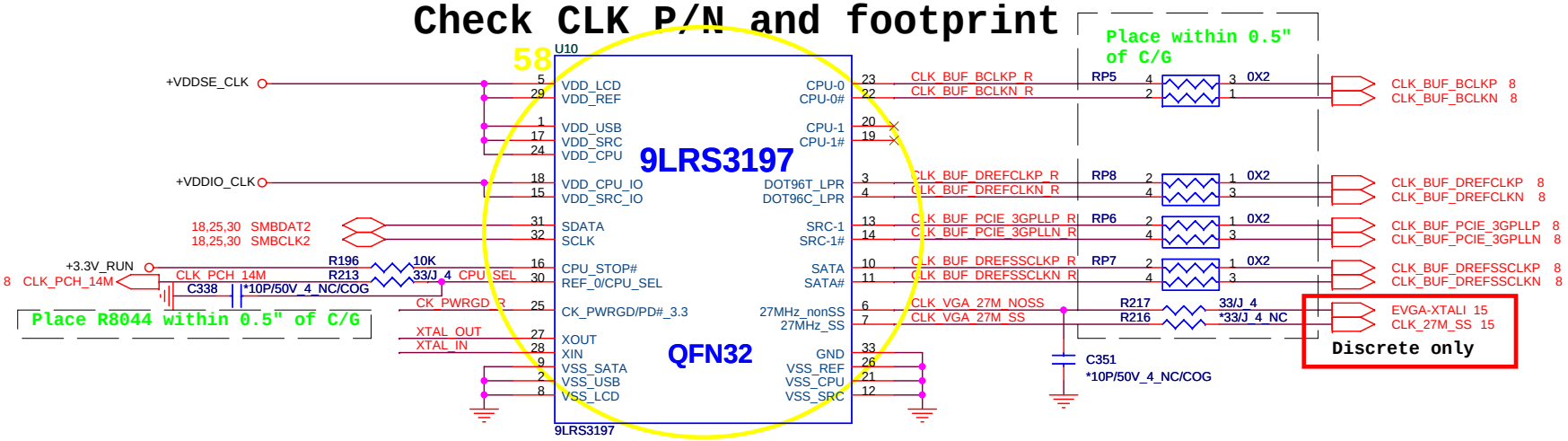
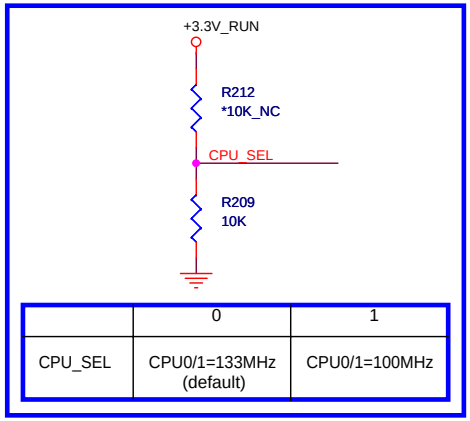


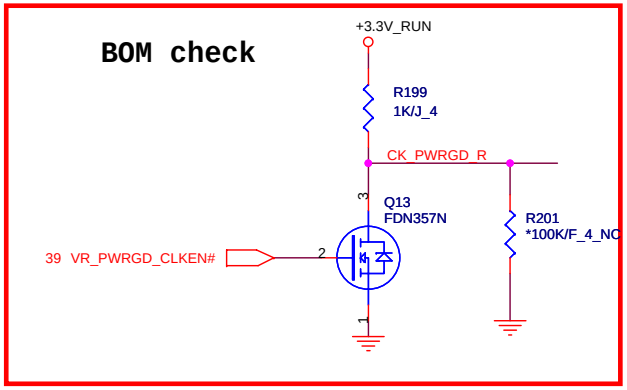
02

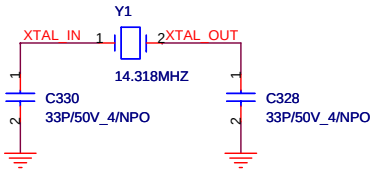
Check CLK P/N and footprint





	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz





SLG: SLG8SP590VTR Seligo QPN: AL8SP590000
SLG: SLG8SP585VTR Seligo QPN: AL8SP585000
RSC: RTM875N-632-VB-GRT Realtek QPN: AL000875002

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PROJECT : UM8B DIS

Size	Document Number	Rev
	Clock Gen(9LRS3197)/HOLES	1A

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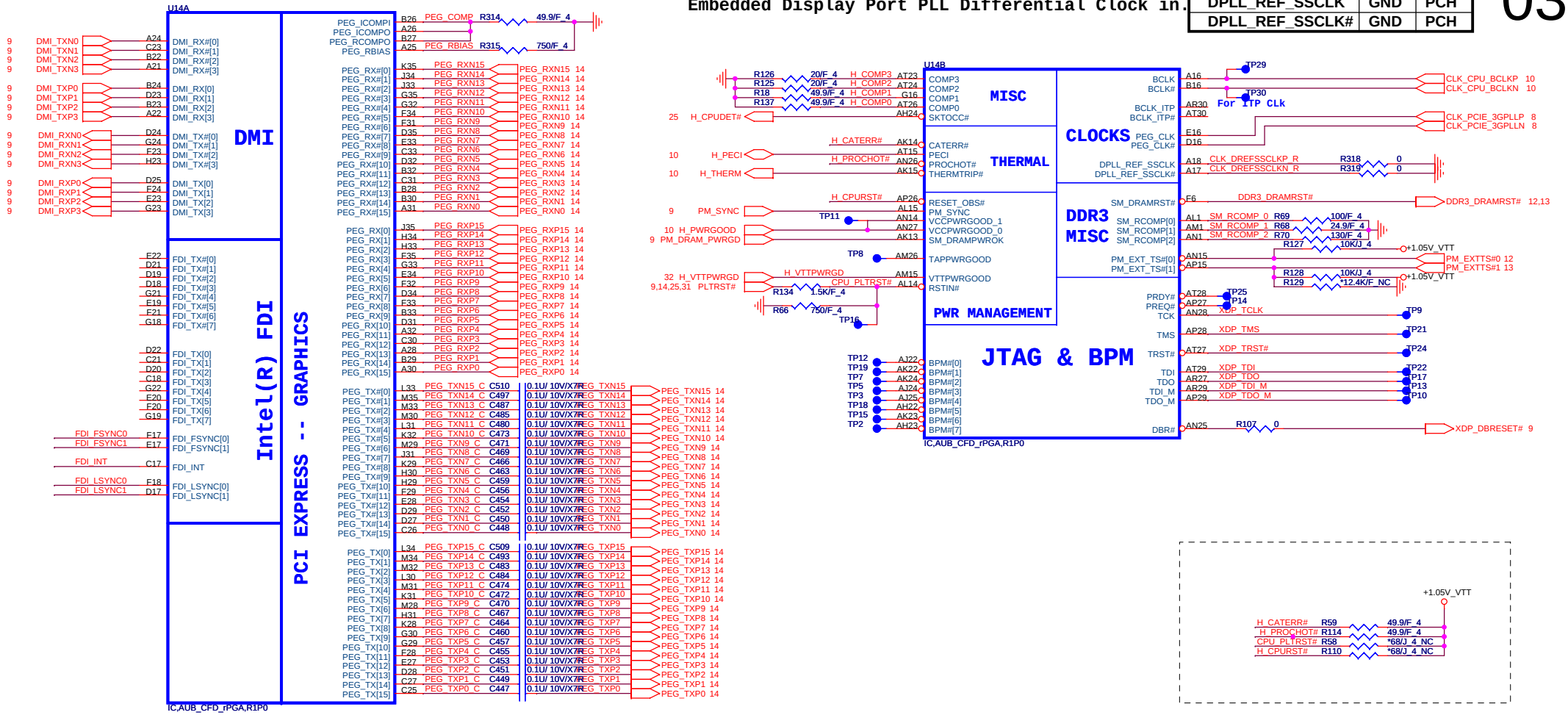
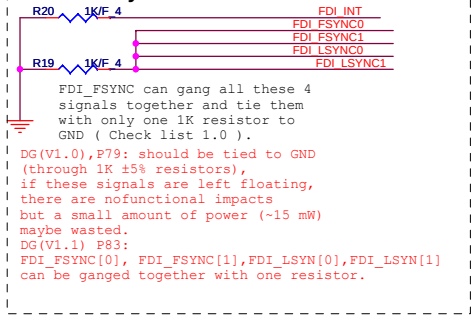
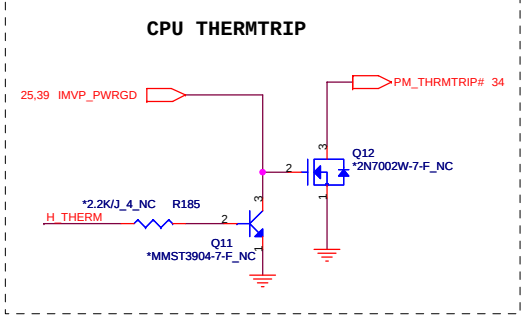
DPLL_REF_SSCLK/DPLL_REF_SSCLK#:
Embedded Display Port PLL Differential Clock in.

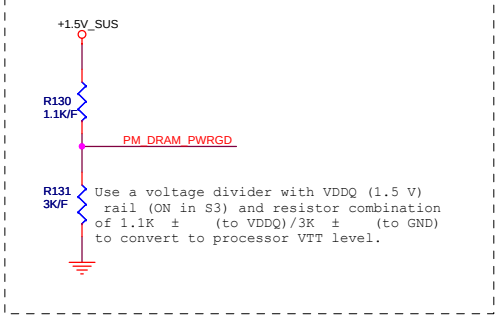
	DIS	UMA
DPLL_REF_SSCLK	GND	PCH
DPLL_REF_SSCLK#	GND	PCH

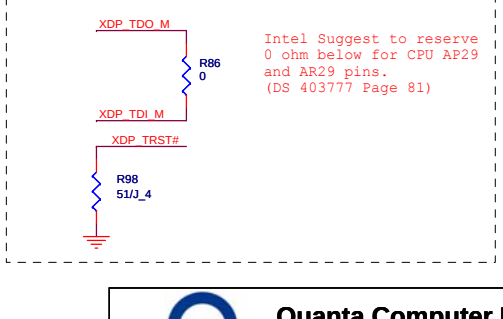
03











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PROJECT : UM8B DIS

Size	Document Number	Rev
	PROCESSER 1/4(HOST&PEX)	1A

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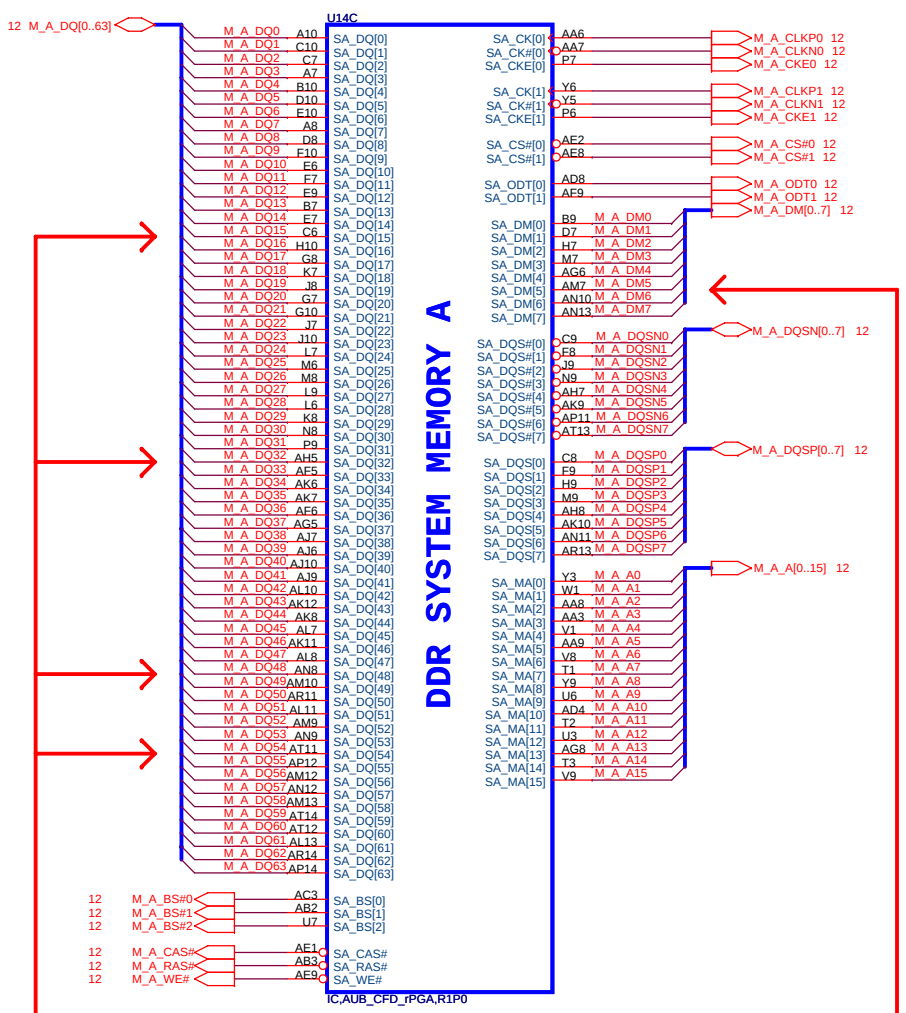
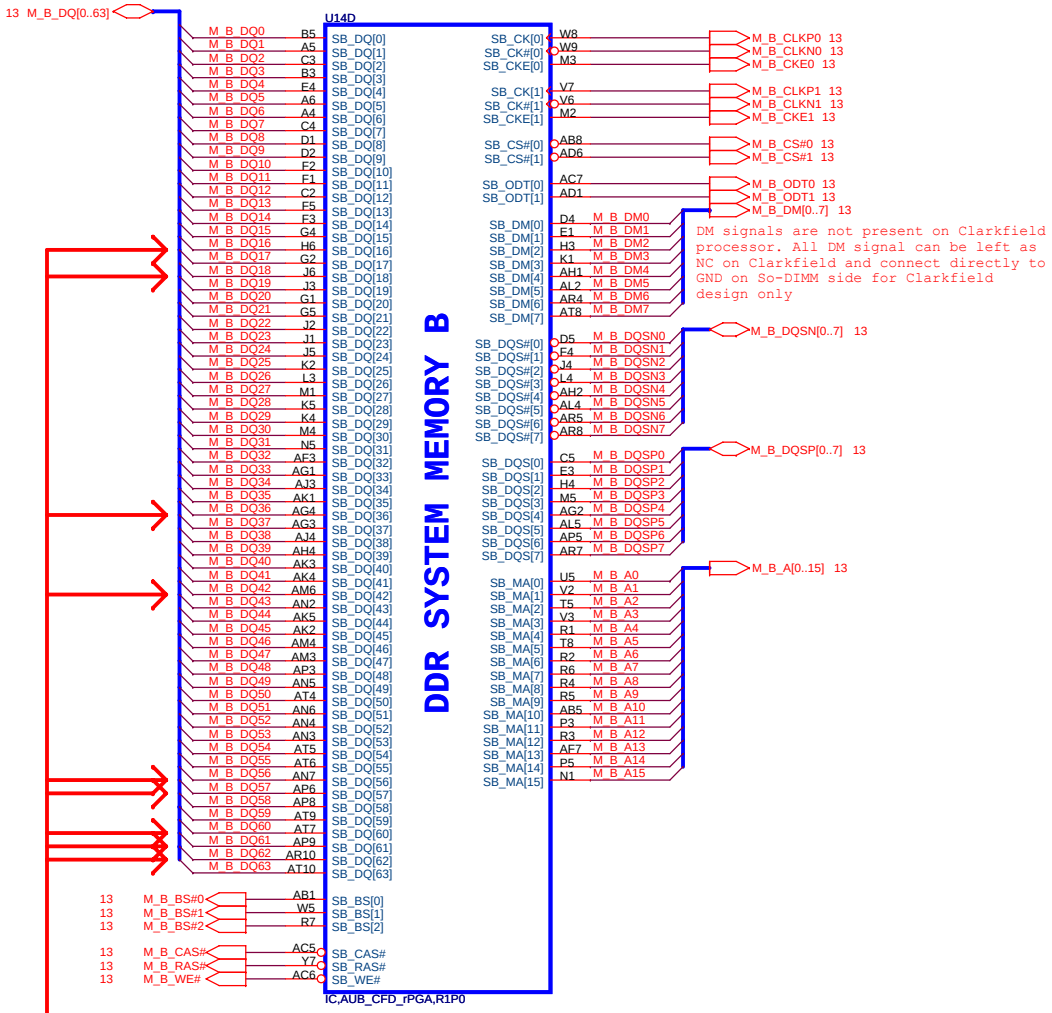
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.



DM signals are not present on Clarkfield processor. All DM signal can be left as NC on Clarkfield and connect directly to GND on So-DIMM side for Clarkfield design only

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

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Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	PROCESSER 2/4(DDR)	1A

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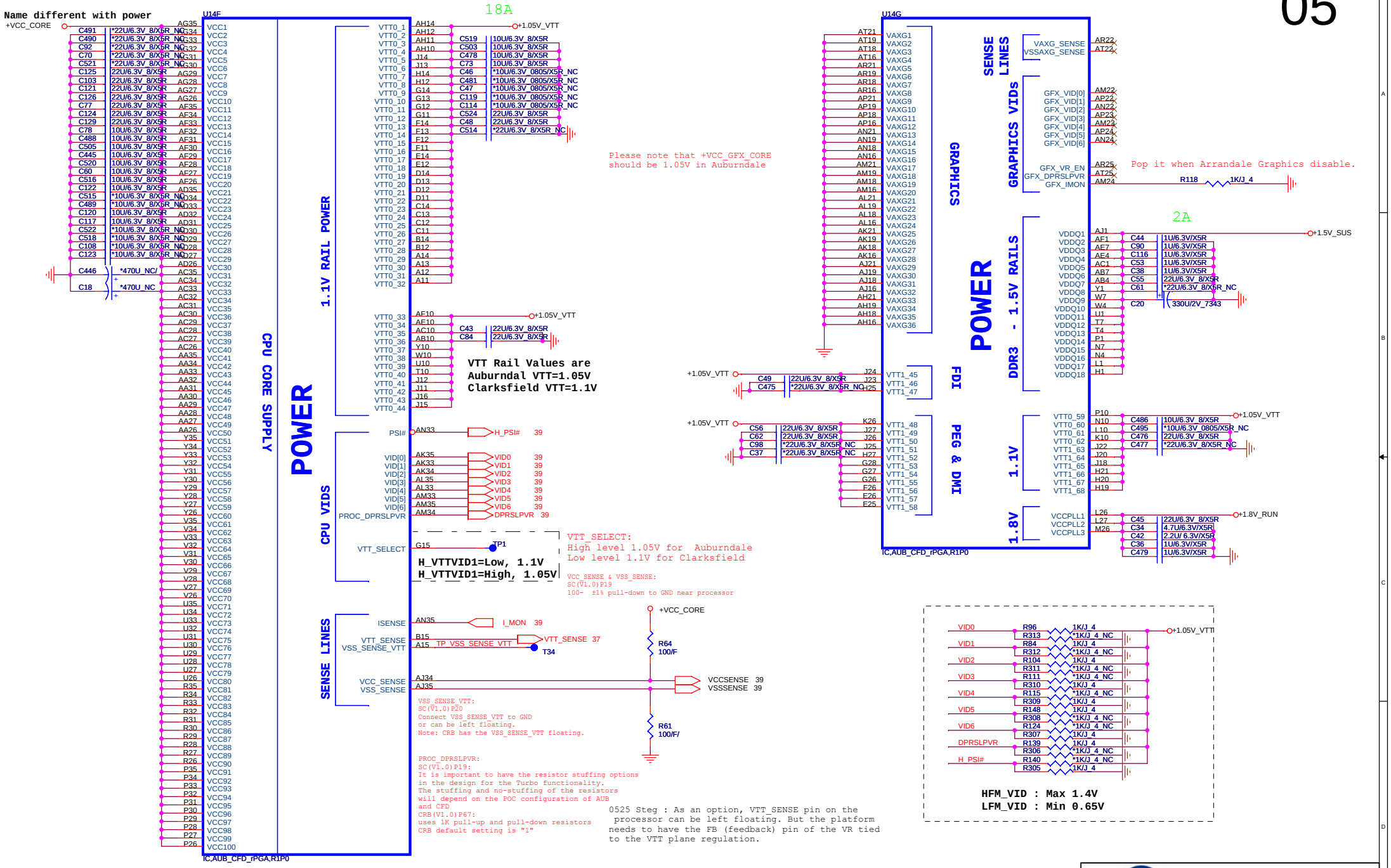

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PROJECT : UM8B DIS

Size	Document Number	Rev
	PROCESSER 3/4(POWER)	1A

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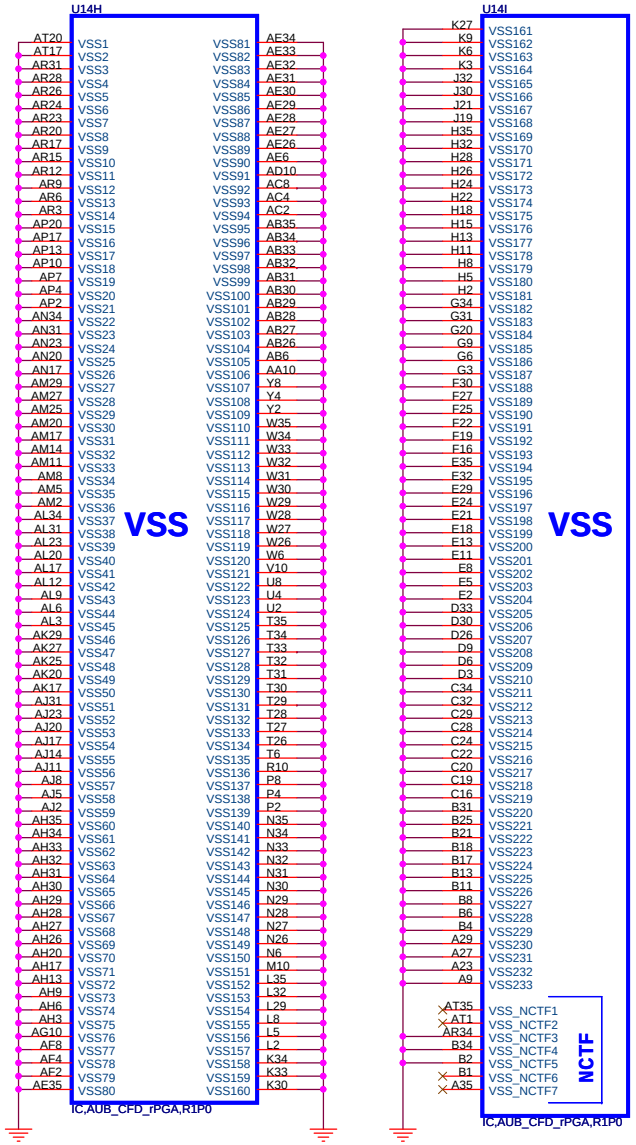
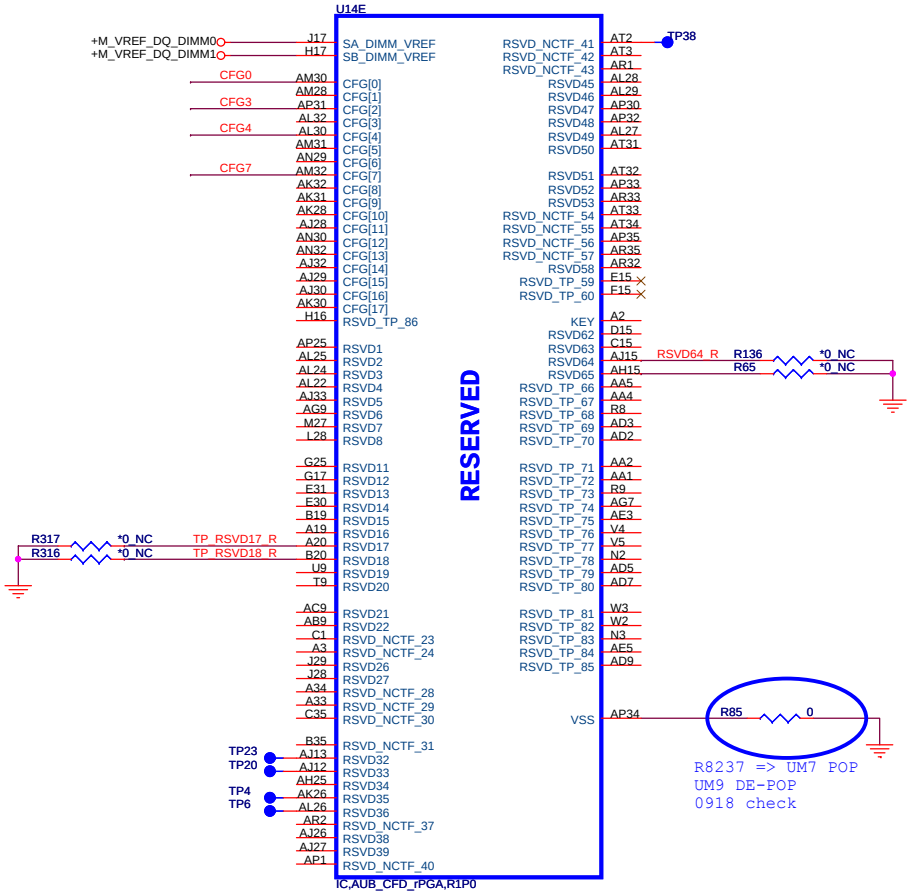
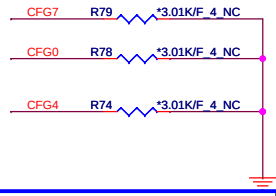
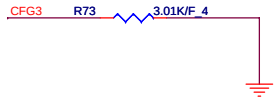
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)







	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

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PROJECT : UM8B DIS

Size	Document Number	Rev
	PROCESSER 4/4 (GND)	1A

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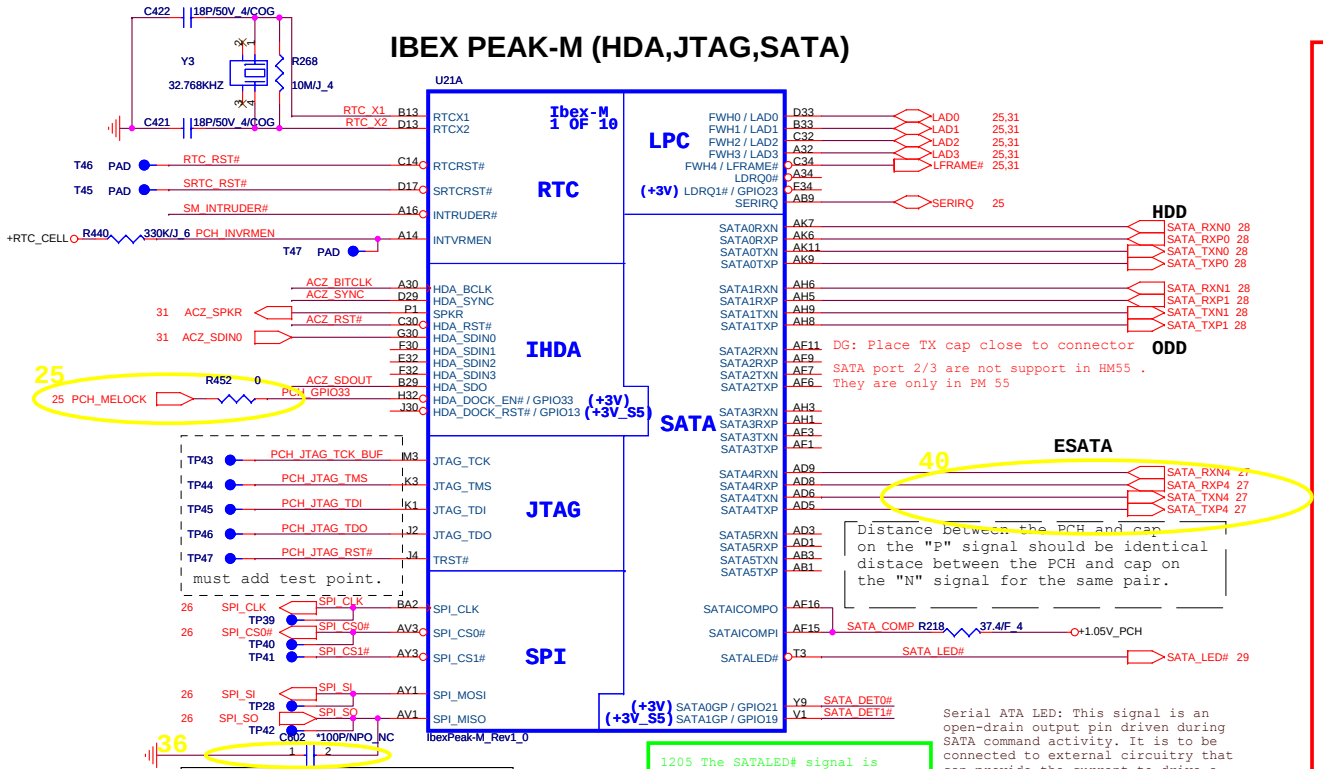
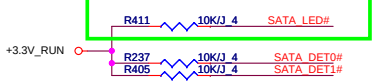
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)



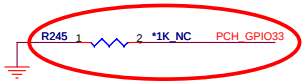
Serial ATA LED: This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required.

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.



Flash Descriptor Security Override

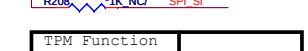
GPIO33	Low = Enabled High = Disabled



(Internal 20K/F pull high to +3.3V_RUN)

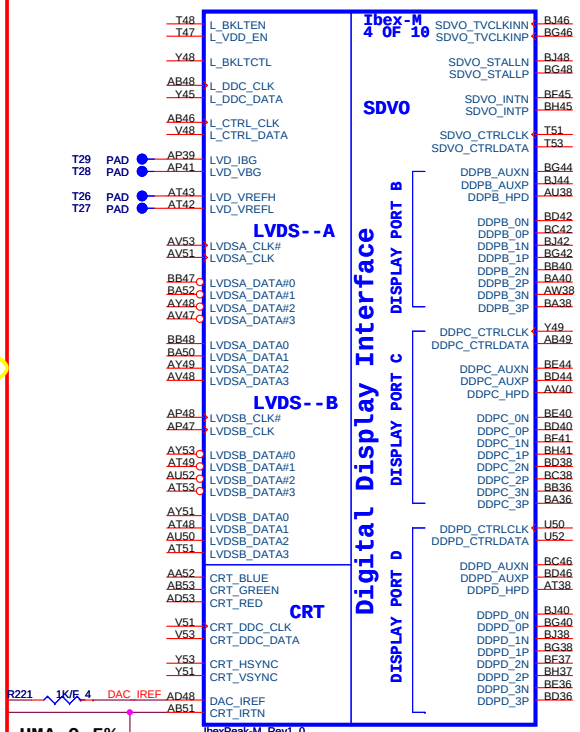
Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

iTPM ENABLE/DISABLE

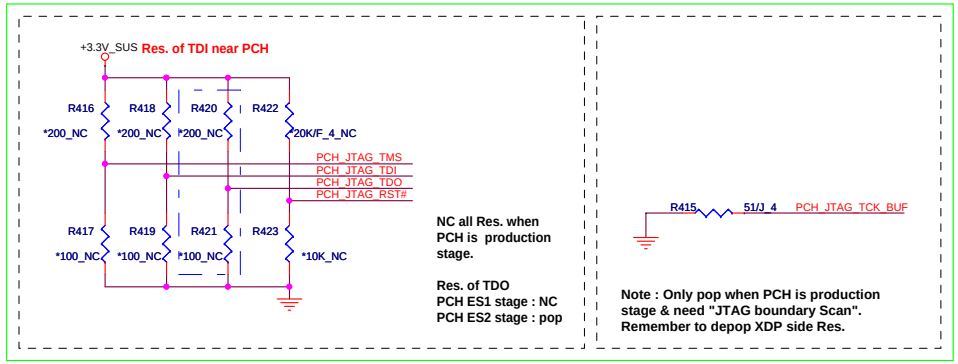


TPM Function	
Enable	Mount
Disable	NC (Default)

UMA CRT,LVDS&HDMI signals
IBEX PEAK-M (LVDS,DDI)



UMA 0.5%
DIS 1%

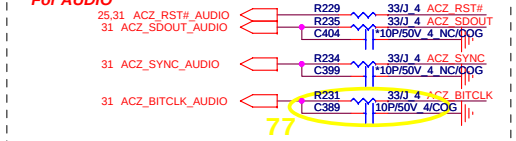


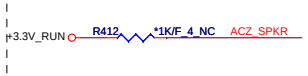
NC all Res. when PCH is production stage.

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

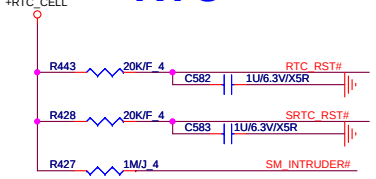
For AUDIO





No Reboot strap.	
SPKR	Low = Default. High = No Reboot.

RTC



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PROJECT : UM8B DIS

Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	1A

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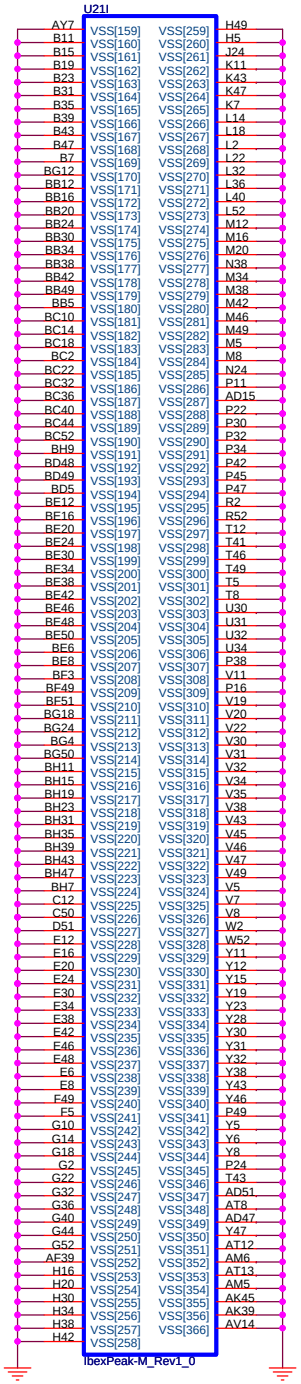
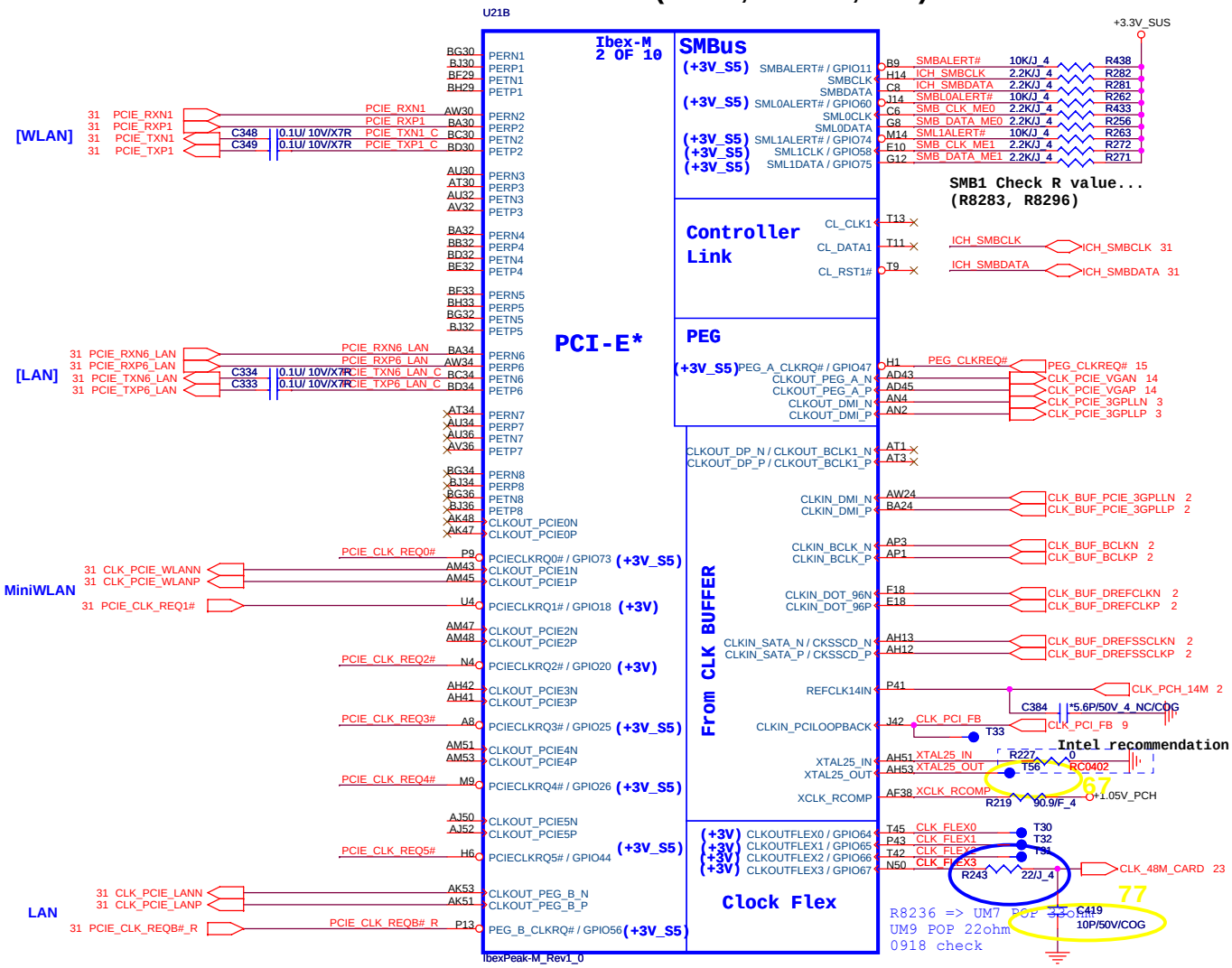
IBEX PEAK-M (GND)



IBEX PEAK-M (PCI-E,SMBUS,CLK)



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PROJECT : UM8B DIS

Size	Document Number	Rev
	PCH 2/5 (PCIE, SMBUS, CK)	1A

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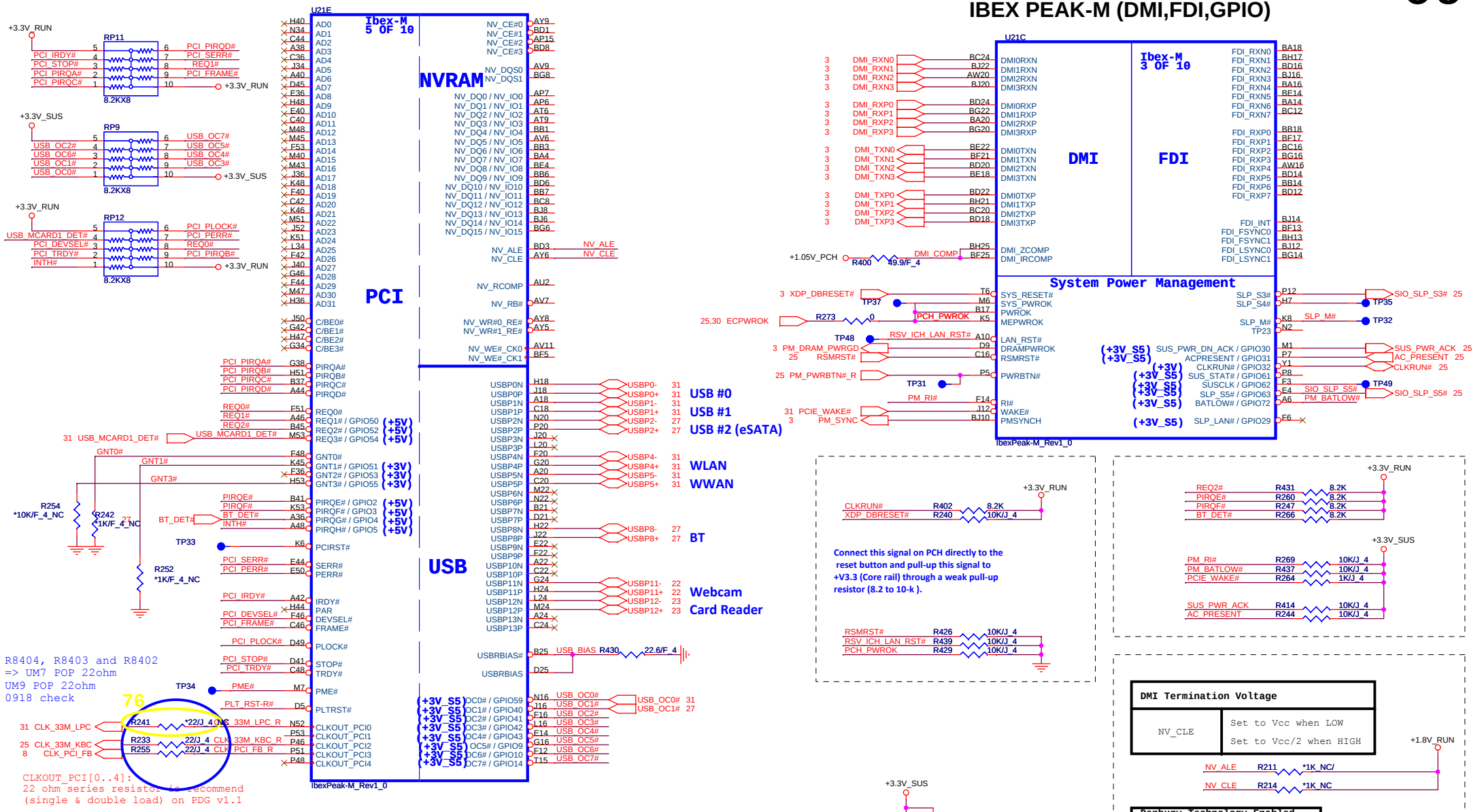
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (DMI,FDI,GPIO)



A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap		
GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

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PROJECT : UM8B DIS

Size	Document Number	Rev
	PCH 3/5 (PCI,ONFI,USB,DMI)	1A

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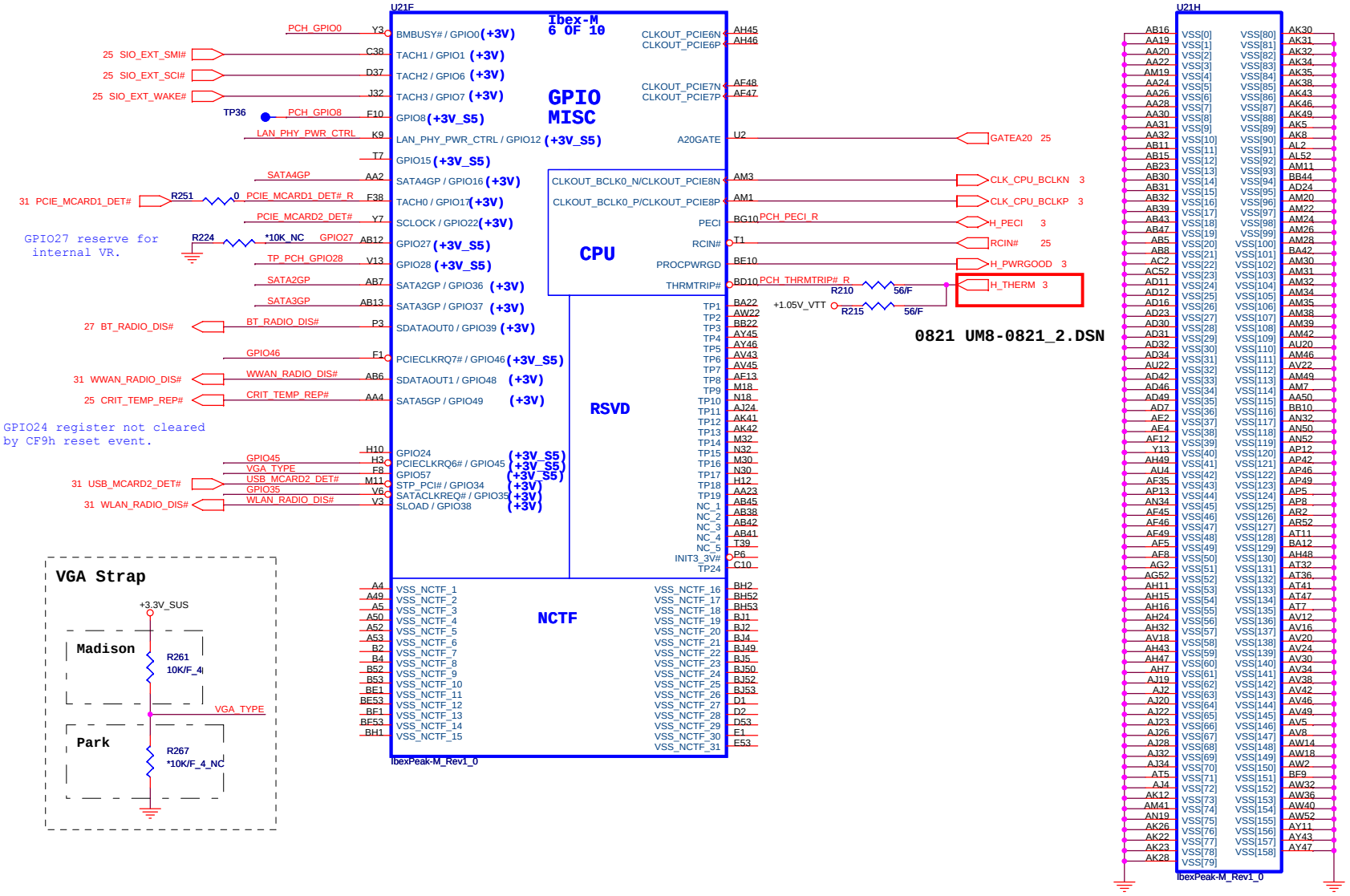
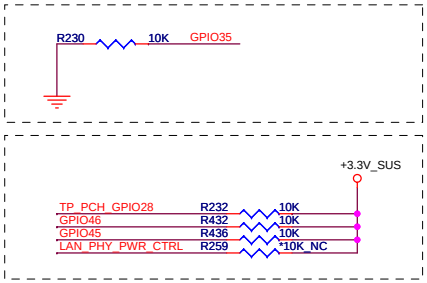
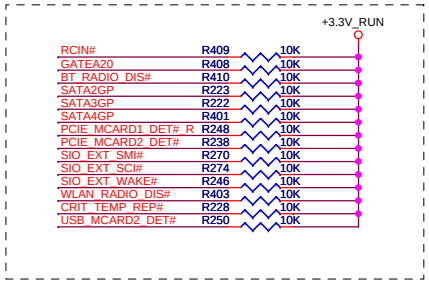
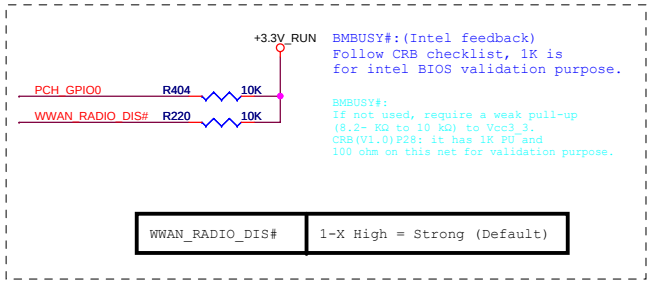
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)









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PROJECT : UM8B DIS

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	1A

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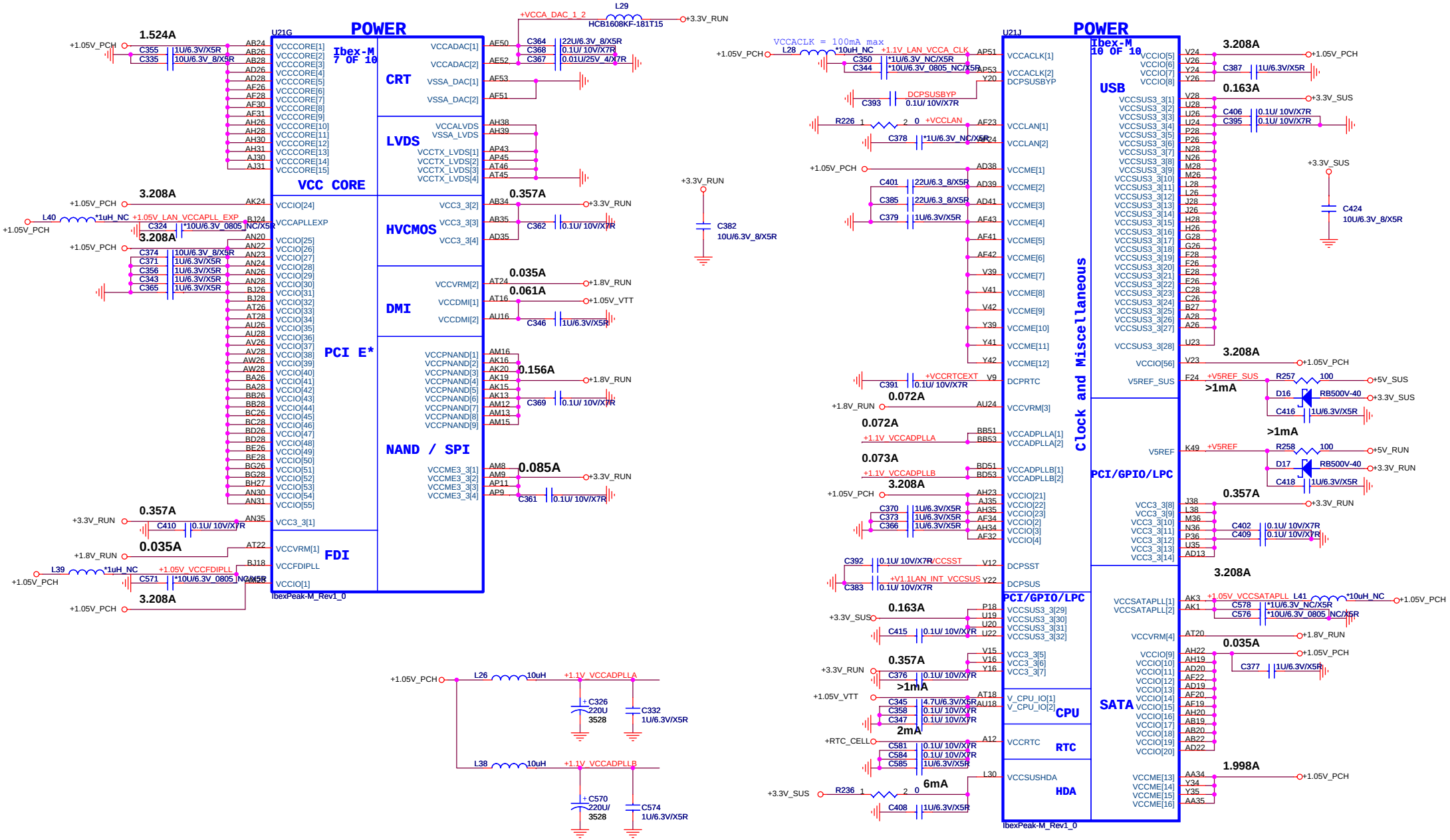
Cap quantities follow UM3



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PROJECT : UM8B DIS

Size	Document Number	Rev
	PCH 5/5 (POWER)	1A

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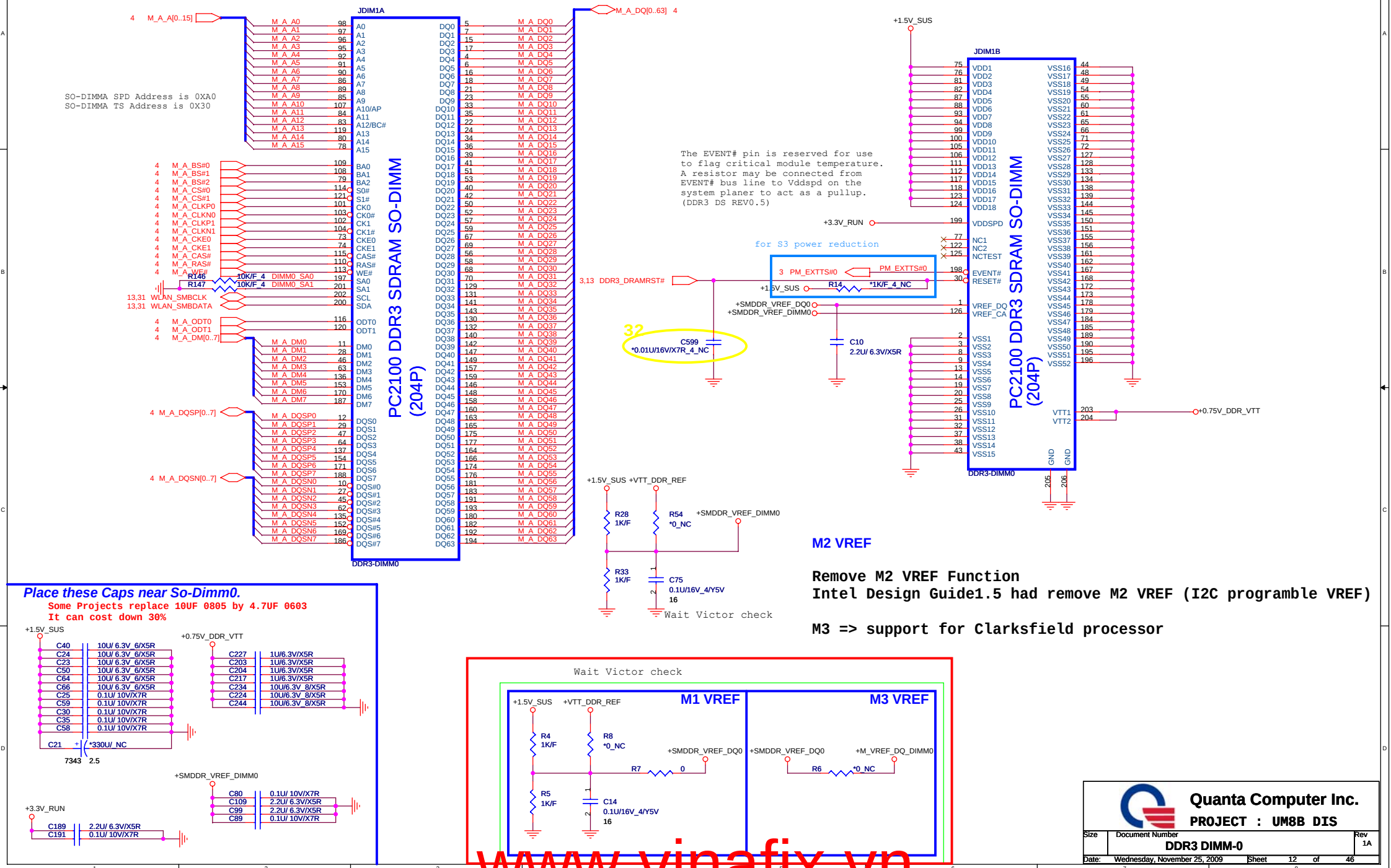

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PROJECT : UM8B DIS

Size	Document Number	Rev
	DDR3 DIMM-0	1A

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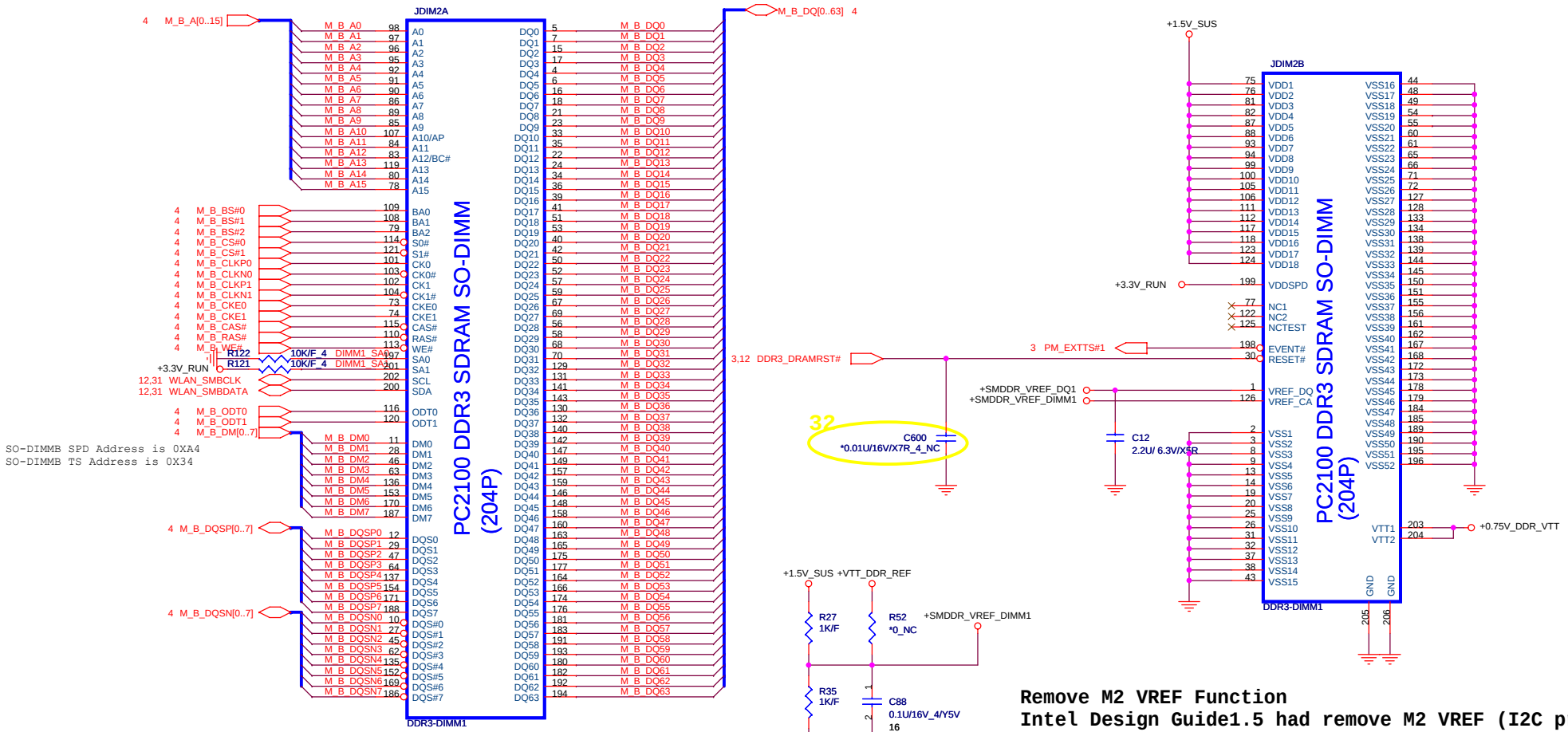
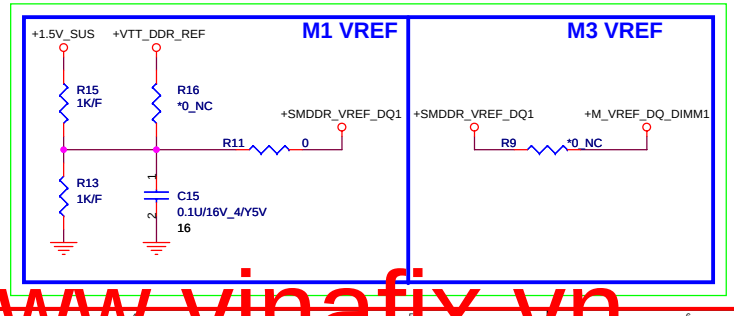


Remove M2 VREF Function
Intel Design Guide1.5 had remove M2 VREF (I2C programble VREF)

M3 => support for Clarksfield processor

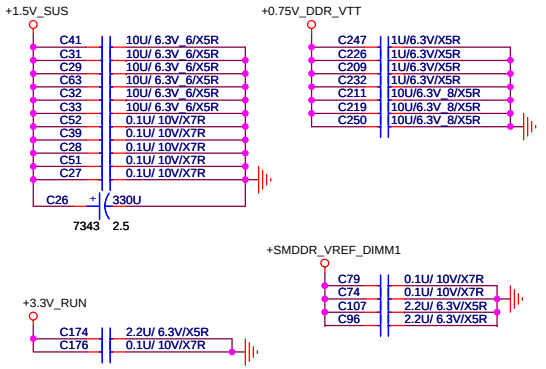
Wait Victor check

for arrandal nc, for clesfied connect



Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



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PROJECT : UM8B DIS

Size	Document Number	Rev
	DDR3 DIMM-1	1A

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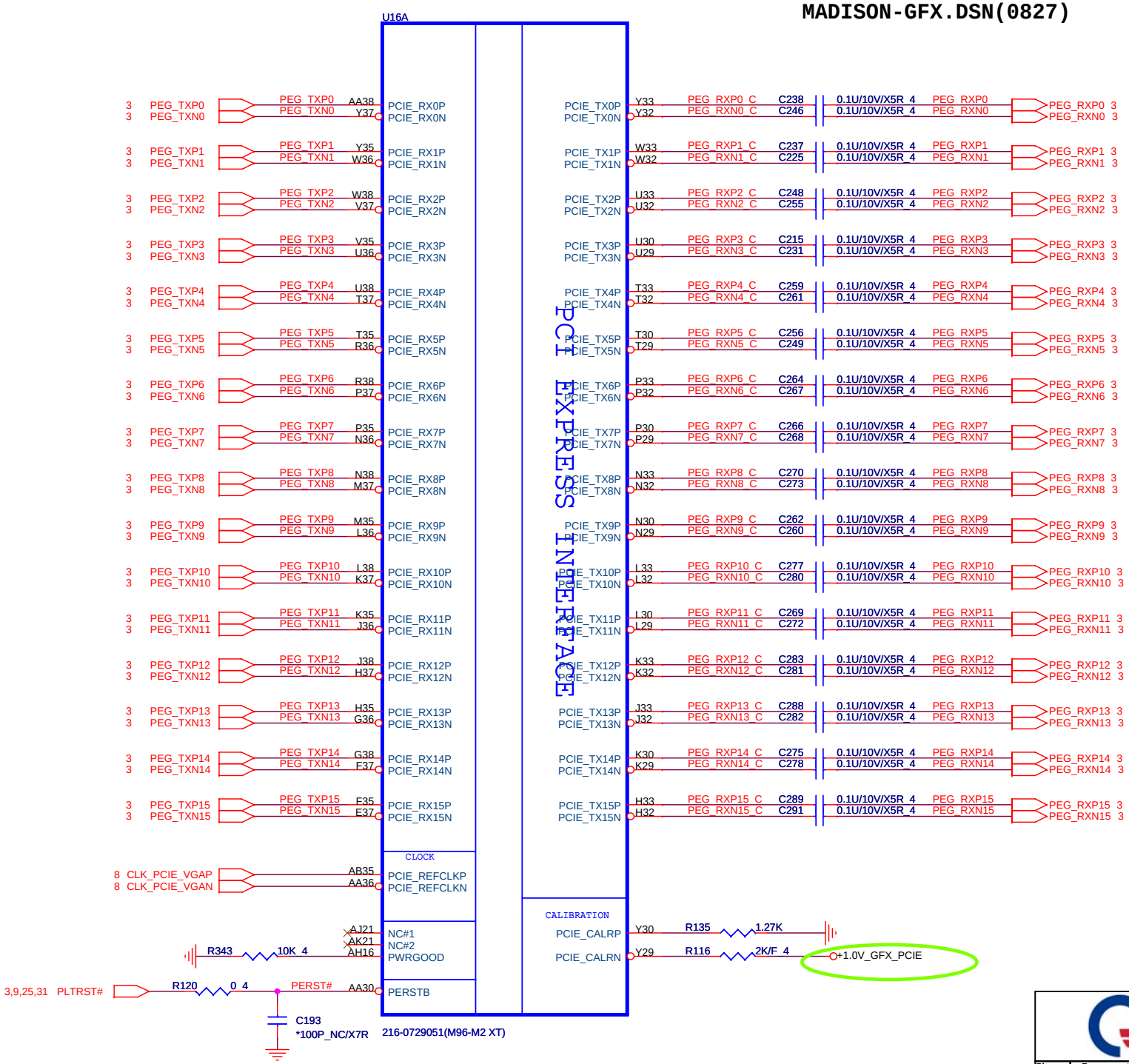

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PROJECT : UM8B DIS

Size	Document Number	Rev
	Madison PCIE I/F	1A

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Memory Straps		RAM_ TYPE_CFG3	RAM_ TYPE_CFG2	RAM_ TYPE_CFG1	RAM_ TYPE_CFG0
800 MHz 1GB(64M*16) Hynix_Orion die	H5TQ1G63BFR-12C	0	0	0	0
800 MHz 1GB(64M*16) Samsung_E die	K4W1G1646E-HC12	0	0	0	1
		0	0	1	0
		0	0	1	1
		0	1	0	0
		0	1	0	1

Note : Required Frequency = 800 MHz

VRAM TYPE

MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0

APERTURE SIZE

CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	0
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	0
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	11
VIP_DEVICE_STRAP_EN	VGAVSYNC2	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0
BIOS_ROM_EN (Internal pull down)	GPIO_22_ROMCSB	1 = Enable external BIOS ROM device 0 = Disable external BIOS ROM device	0

Park and Madison

!!! NC when PARK-M2

(GPIO_19_CTF)
Critical temperature fault (active high)
CTF will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the motherboard can protect the ASIC from damage by removing power.

GPU Power-on sequence

1 => +3V_D
2 => +1.5V_GPU = +1.5V_RUN
3 => +VGPU_CORE
4 => +VGPU_IO
5 => +1V = +1.0V_GFX_PCIE
6 => +1.8V_GPU = +1.8V_RUN_GFX
7 => dGPU_PWROK

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

1.0V @ 150mA DPLL_VDDC

(1.8V @ 120mA DPLL_PVDD)

(1.8V @ 20mA TSVDD)

Layout Note: Place 150 ohm termination resistors close to ATI CHIP.

(1.8V @ 70mA AVDD)

(1.8V @ 45mA VDD1DI)

(1.8V @ 40mA VDD2DI)

(1.8V @ 20mA A2VDDQ)

HDMI

LVDS

CRT

For Park,Madison production version ASIC is need removed workaround.

Park
pre-production build could get the "ENG" marking.

Madison
- date codes up to 0941 are NOT Production Samples
- date codes from 0942 and up are Production Samples

Solve Intermittent System Boot-up Hangs

DDC6CLK/DDC6DATA support internal HDCP(High-bandwidth Digital Content Protection) function.

216-0729051(M96-M2 XT)

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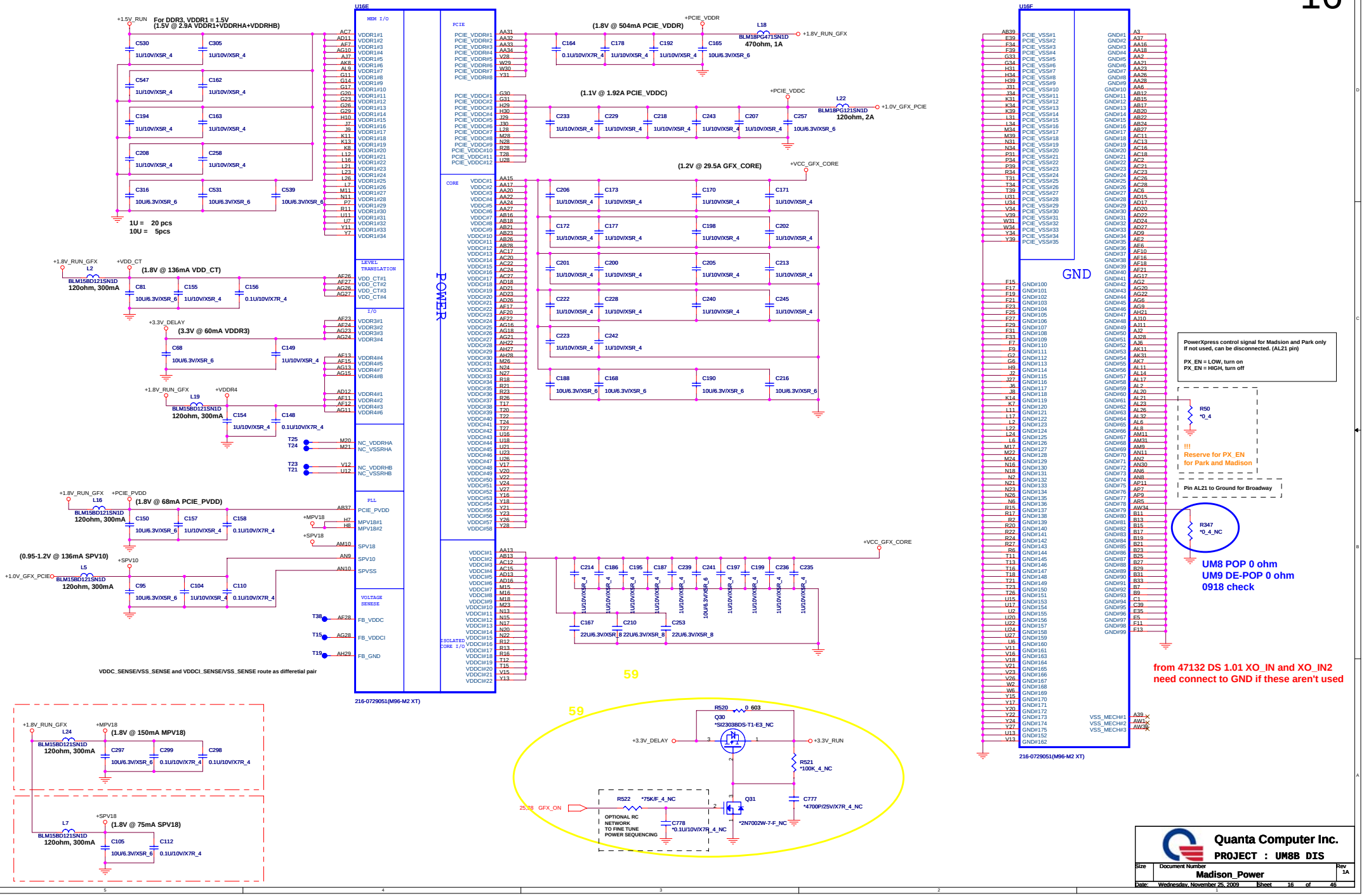
Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	Madison_IO&STRAP	1A

Date: Wednesday, November 25, 2009 Sheet 15 of 46



Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	Madison_Power	1A

Date: Wednesday, November 25, 2009 Sheet 16 of 46

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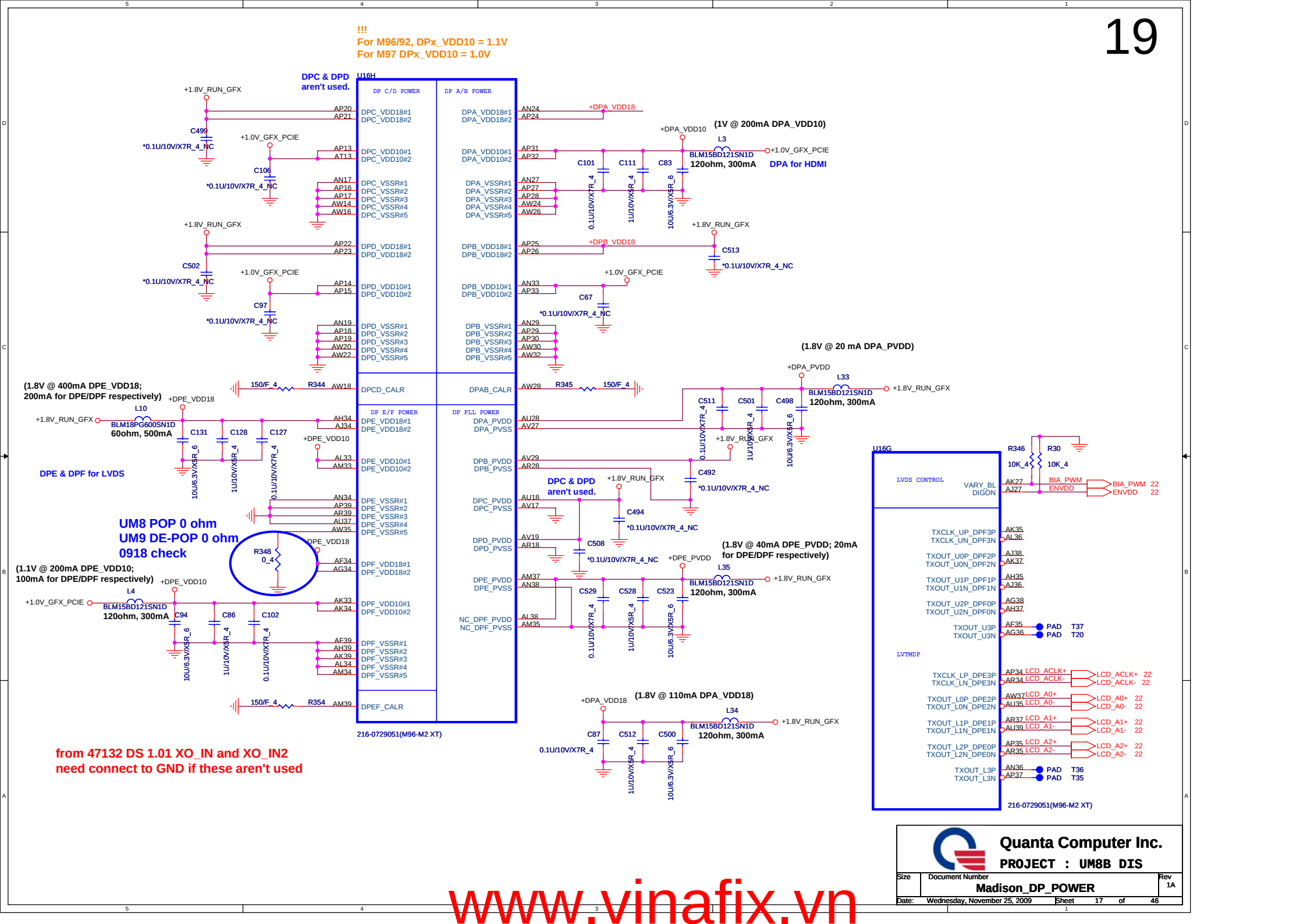

Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	Madison_DP_POWER	1A

Date: Wednesday, November 25, 2009 Sheet 17 of 46

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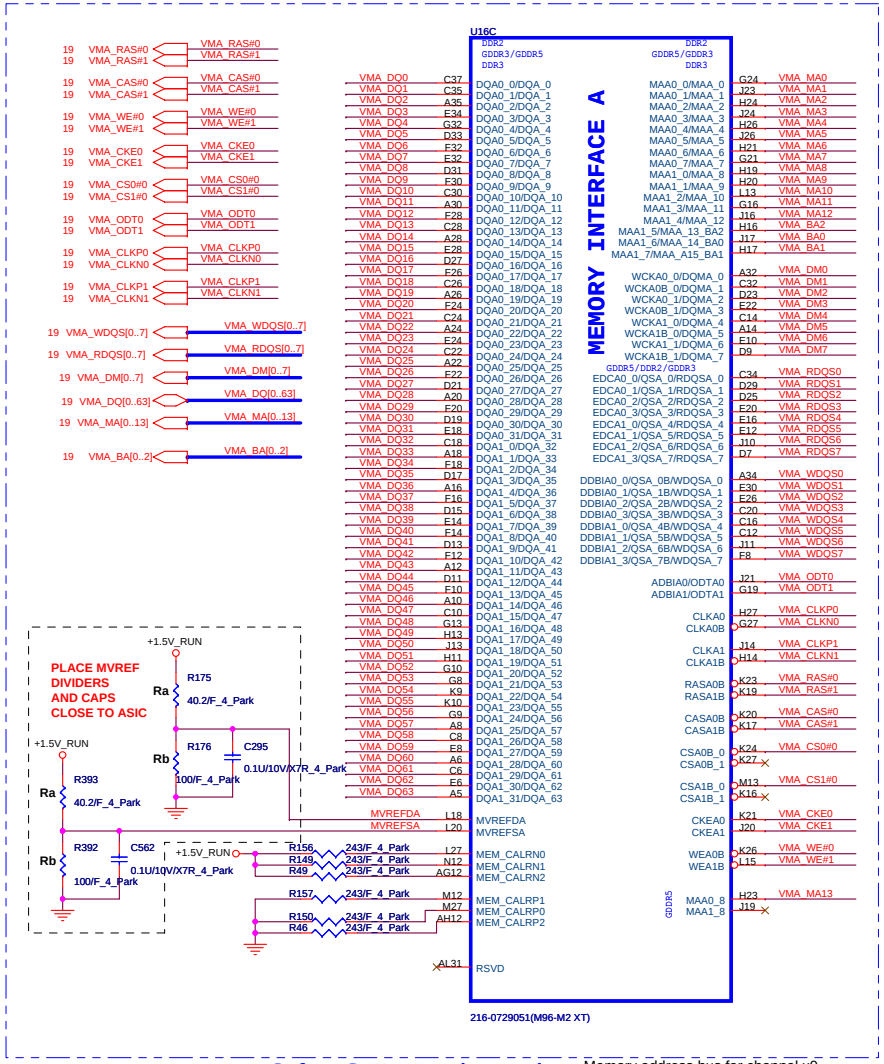
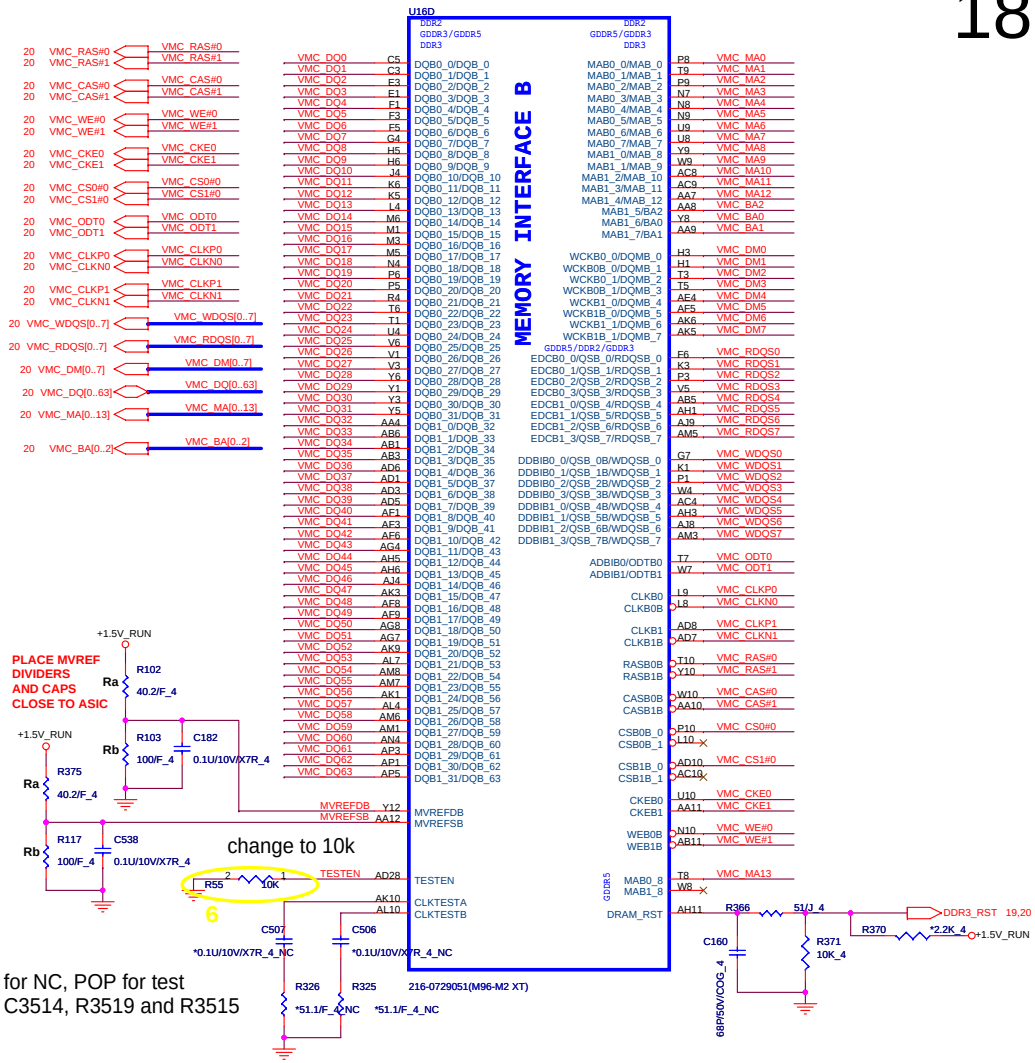




Normal for NC, POP for test
C3513, C3514, R3519 and R3515

NC for GFX Park portion

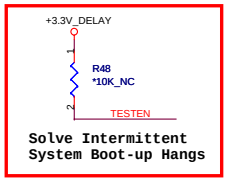
For Park,Madison production version ASIC is need removed workaround.

Park
pre-production build could get the "ENG" marking.

Madison
- date codes up to 0941 are NOT Production Samples
- date codes from 0942 and up are Production Samples

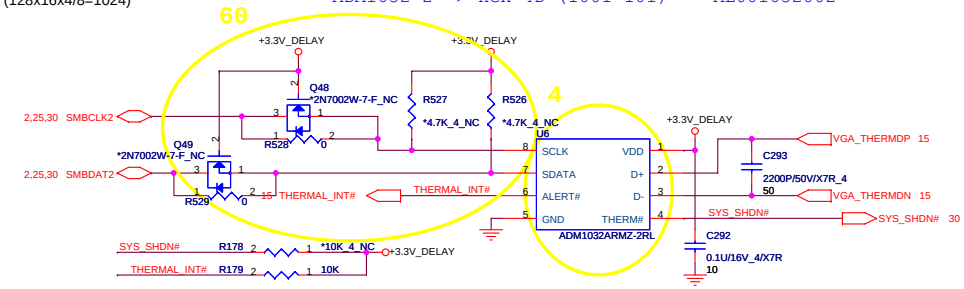
Memory address bus for channel x0. Provides multiplexed row and column addresses. For 128-Mbit x16 DDR3 support, MAx13 is supported on MAx0_8. (128x16x4/8=1024)

ADM1032-1 => Hex 4C (1001 100) AL001032001
ADM1032-2 => Hex 4D (1001 101) AL001032002



DDR3/GDDR3 Memory Stuff Option

	GDDR3	DDR3
MVDDQ	1.5V/1.8V	1.5V
Ra	40.2R	40.2R
Rb	100R	100R



Designator	For M97-M2	For Madison
R272	10K	10K
R271	0R/Short	680R
R273	NC	NC
C408	2.2nF	68pF

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	Madison_MEMORY/THERM	1A

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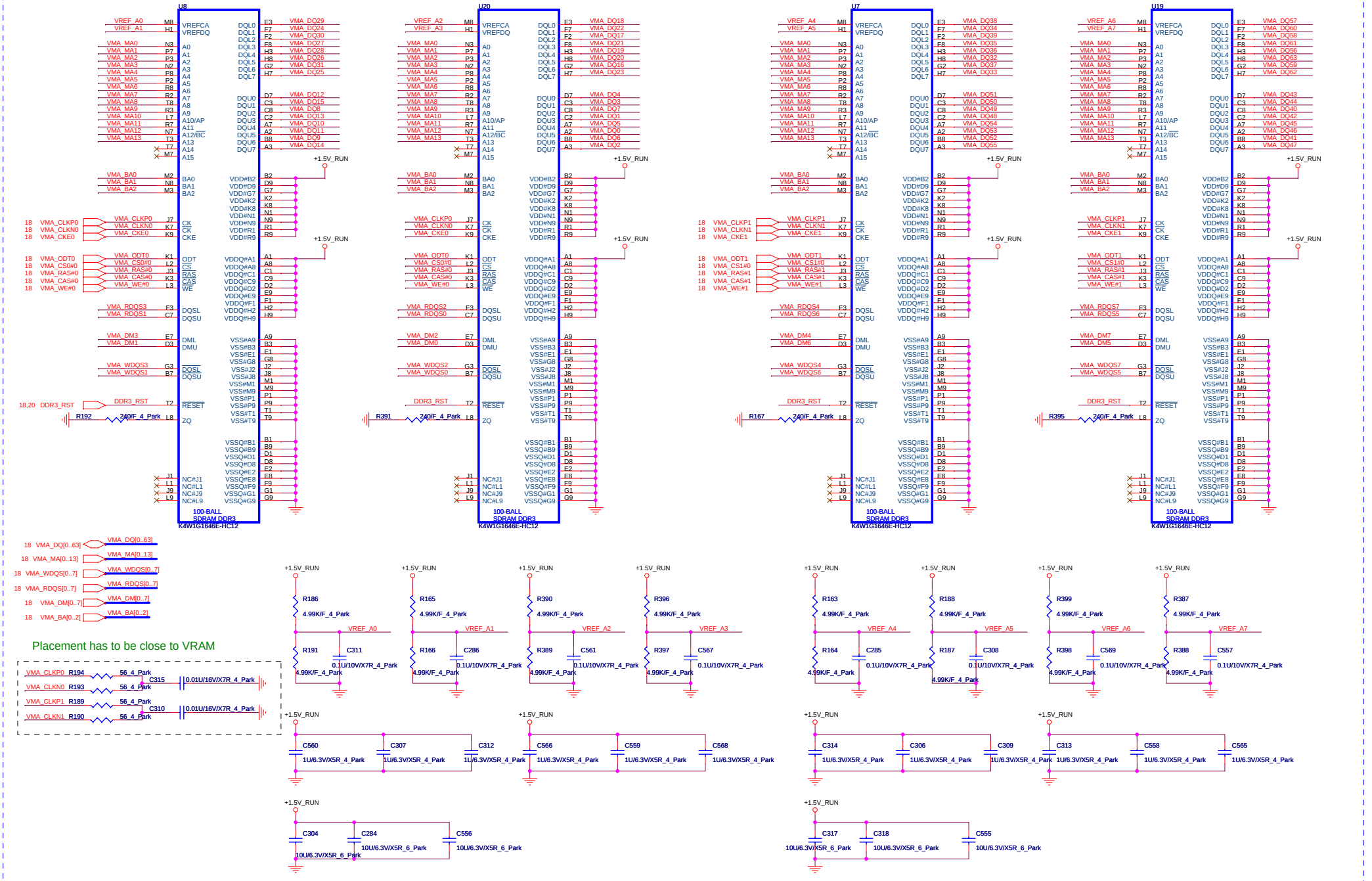
CHECK PN

DDR3 64MX16, CH A : 512MB



NC for GFX Park portion

Samsung: AKD5LGGT505
Hynix: AKD5LZGTW03

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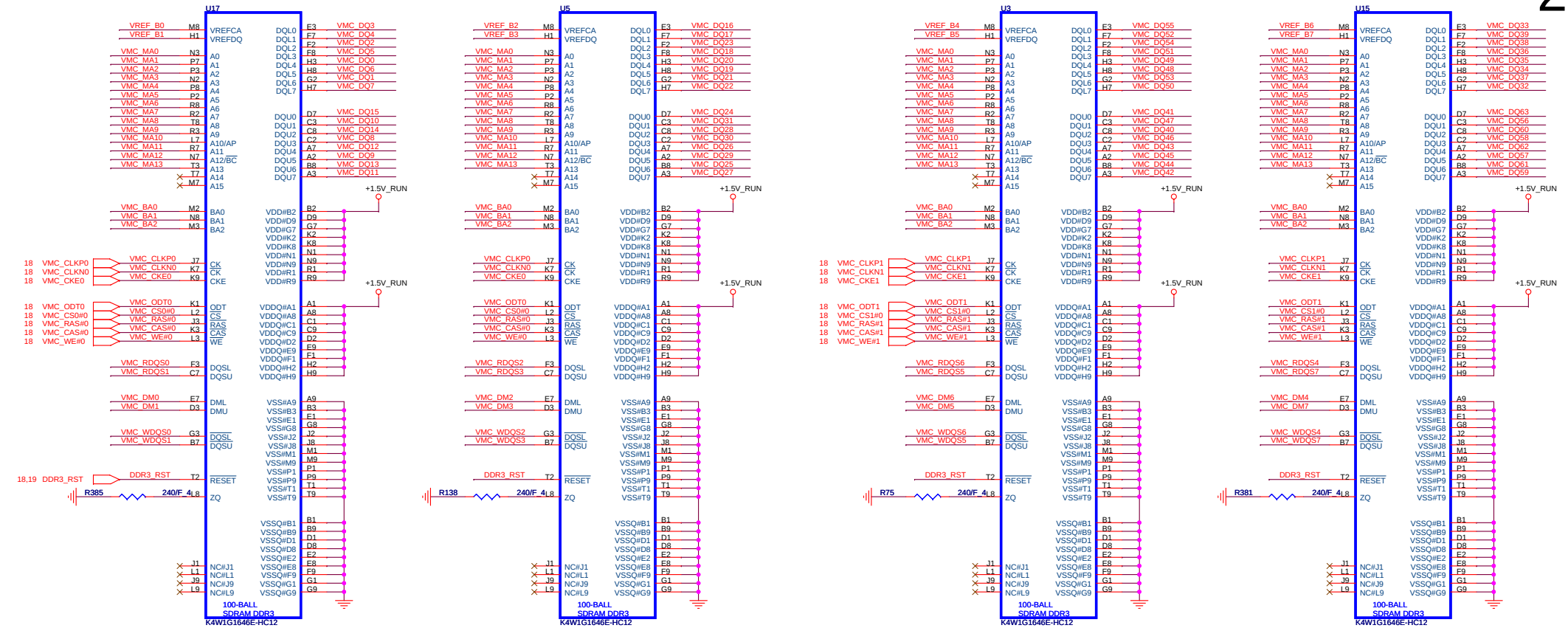
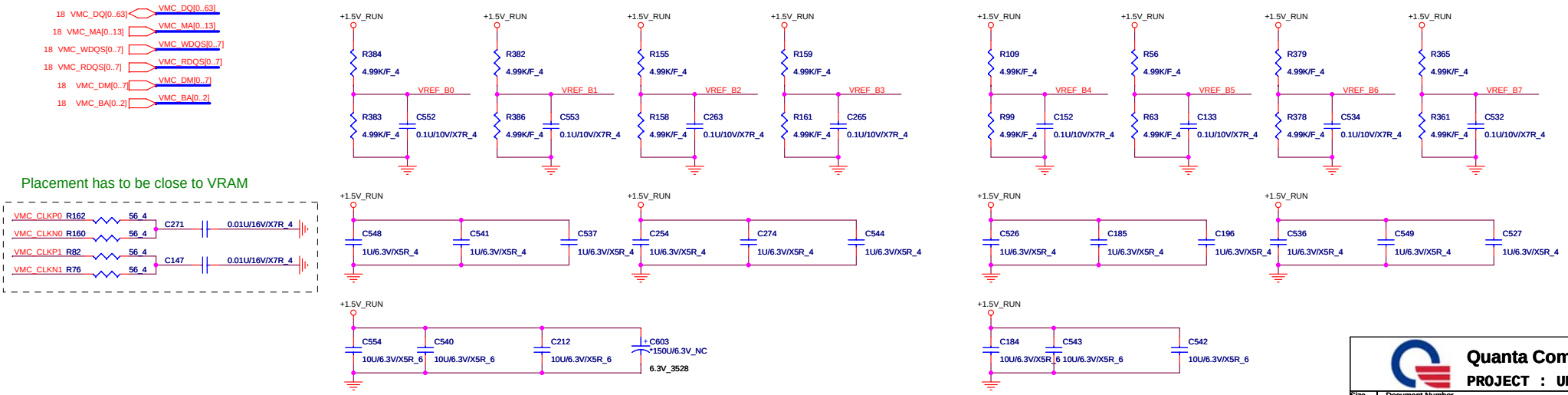
PROJECT : UM8B DIS

Size	Document Number	Rev
	Madison_DDR3_A_512M	1A

Date: Wednesday, November 25, 2009 Sheet 19 of 46

DDR3 64MX16, CH B : 512MB





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PROJECT : UM8B DIS

Size	Document Number	Rev
	Madison_DDR3_B_512M	1A

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Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	Blank	1A

Date: Wednesday, November 25, 2009 Sheet 21 of 46

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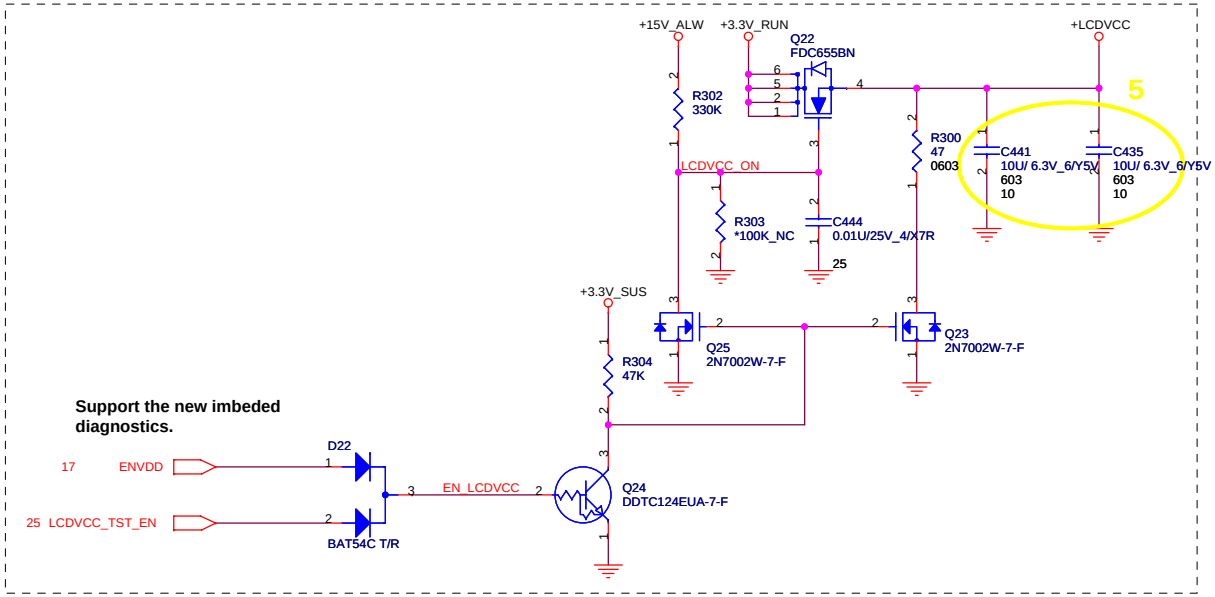

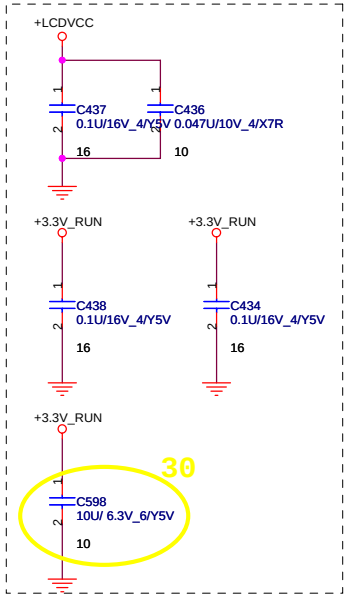

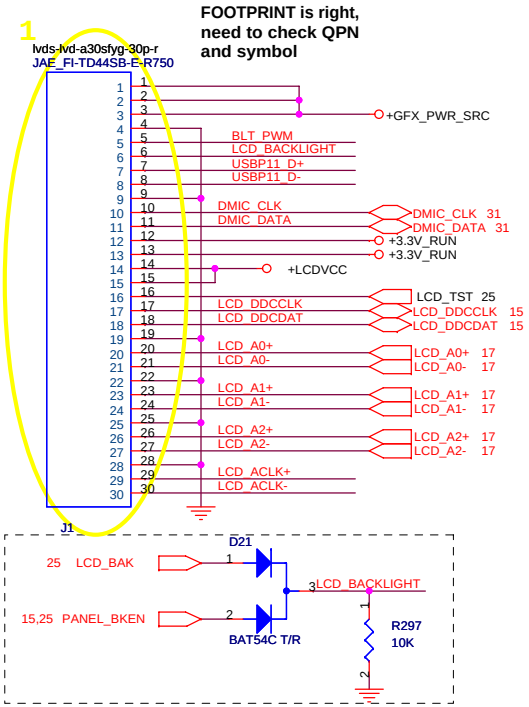

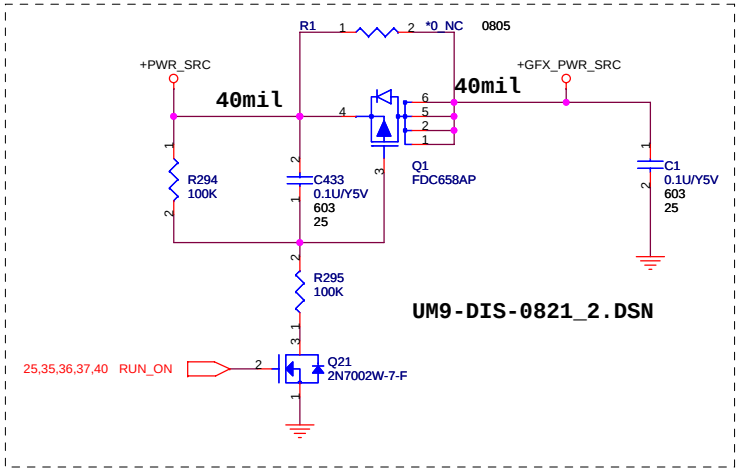

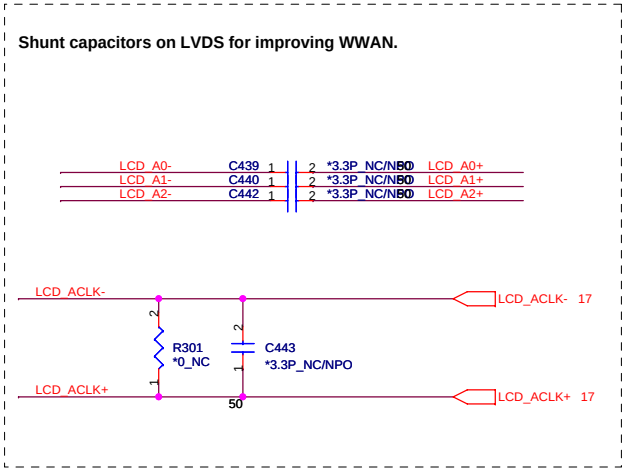

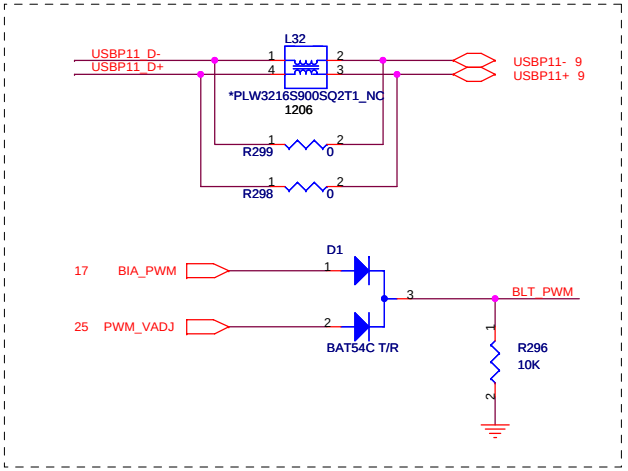

Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	LCD CONN	1A

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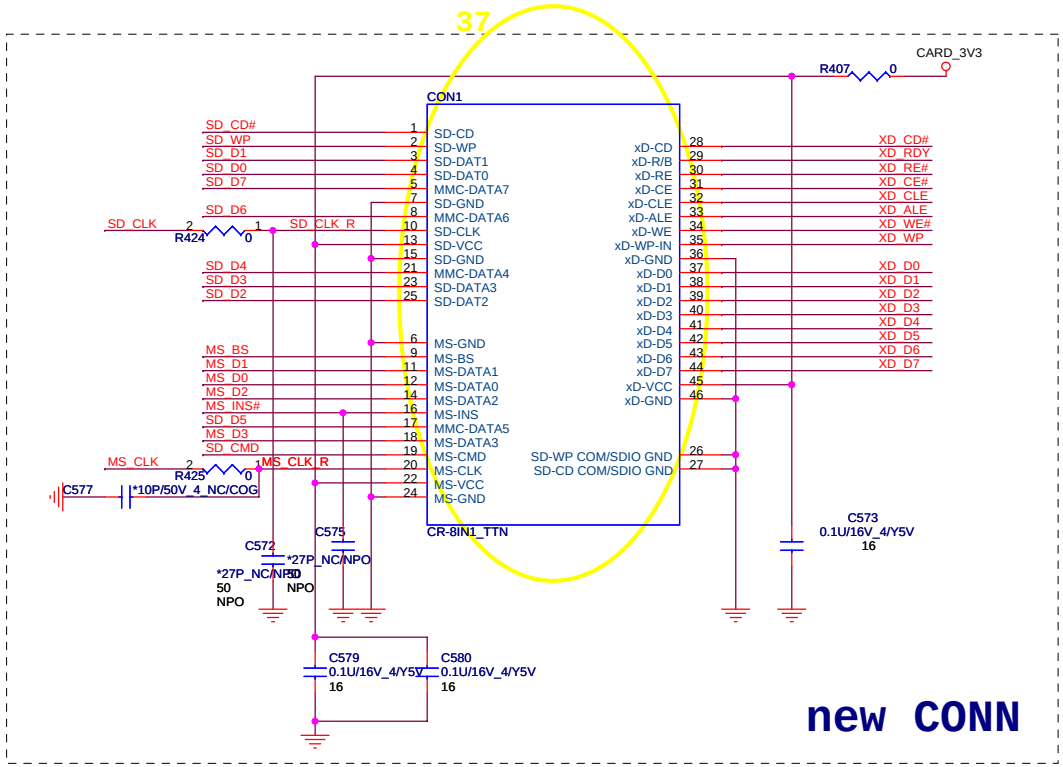
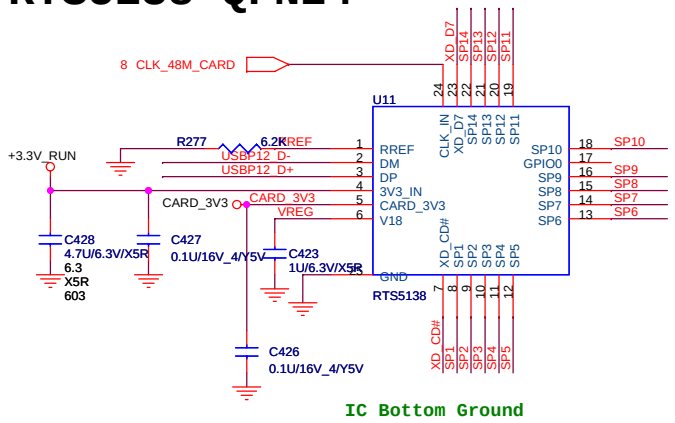


new CONN

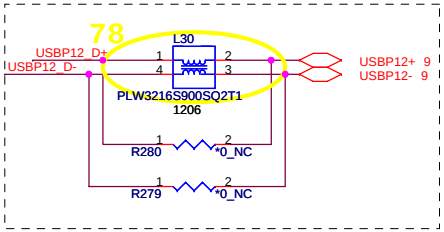
RTS5138-QFN24



IC Bottom Ground

SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS

Share Pin



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PROJECT : UM8B DIS

Size	Document Number	Rev
	Card Reader(RST5138)	1A

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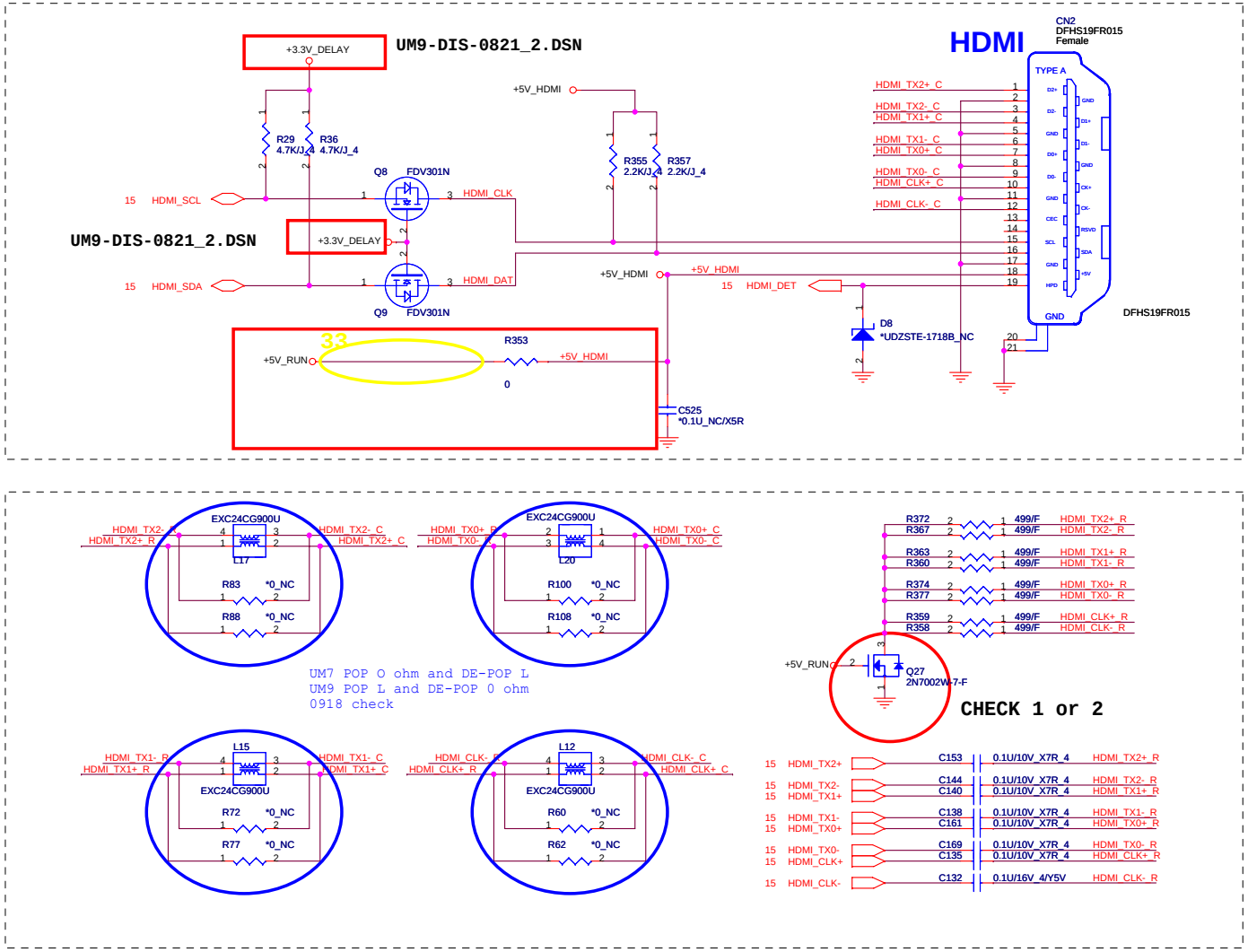

Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	HDMI	1A

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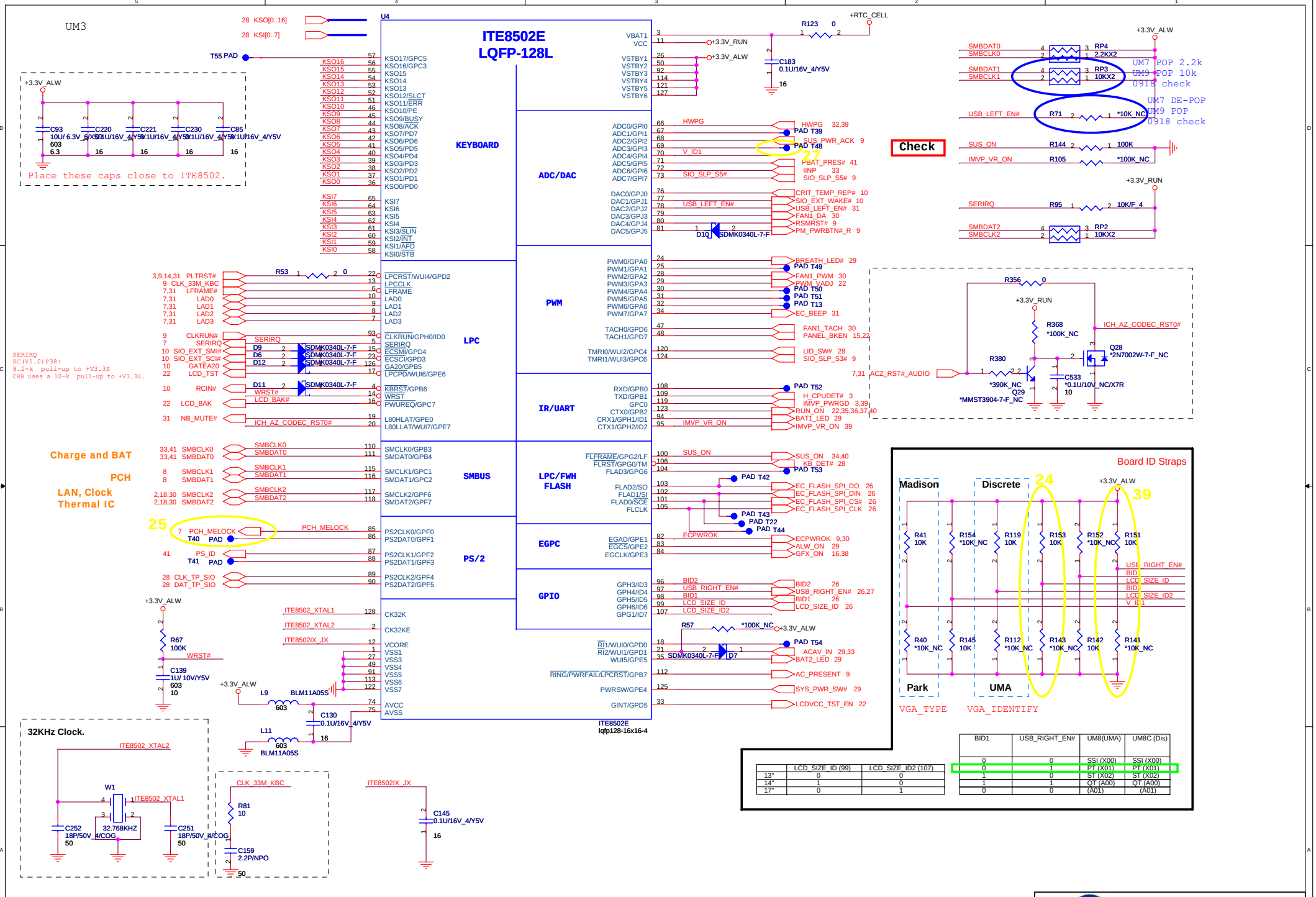

	LCD_SIZE_ID (99)	LCD_SIZE_ID2 (107)
13"	0	0
14"	1	0
17"	0	1

BID1	USB_RIGHT_EN#	UM8(UMA)	UM8C (Dis)
0	0	SSI (X00)	SSI (X00)
0	1	PT (X01)	PT (X01)
1	0	ST (X02)	ST (X02)
1	1	QT (A00)	QT (A00)
0	0	(A01)	(A01)

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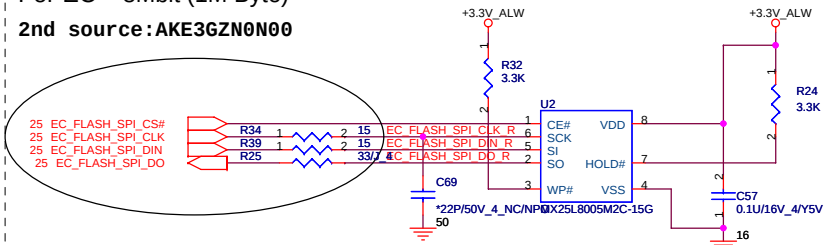
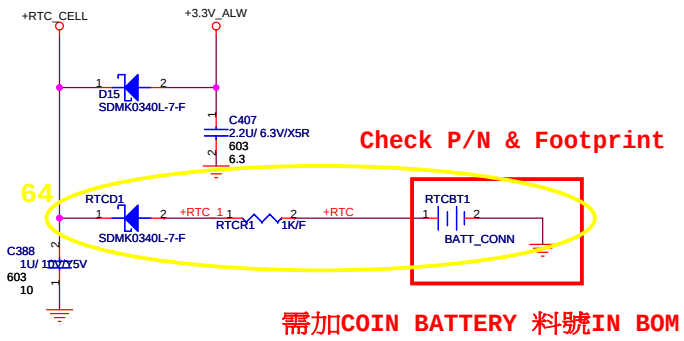
For EC 8Mbit (1M Byte)

2nd source:AKE3GZN0N00



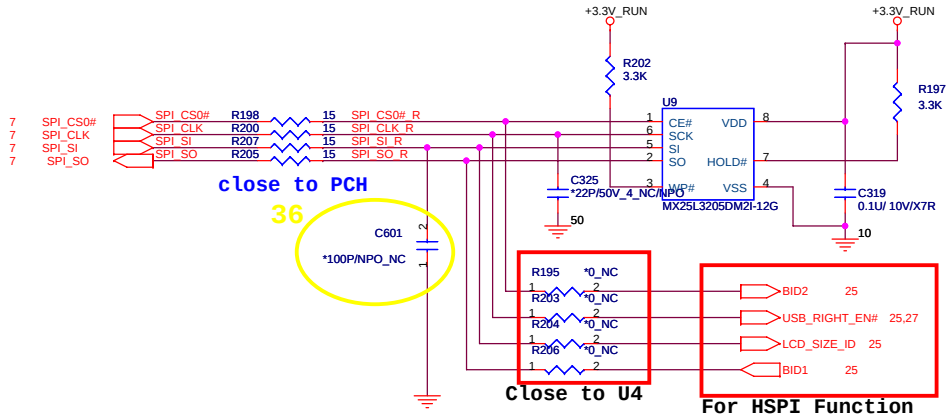
RTC BATTERY



For PCH

32Mbit (4M Byte)

2nd source:AKE39ZP0N00



Quanta Computer Inc.	PROJECT : UM8B DIS	
Size	Document Number: FLASH/RTC	Rev 1A
Date: Wednesday, November 25, 2009	Sheet 26 of 46	

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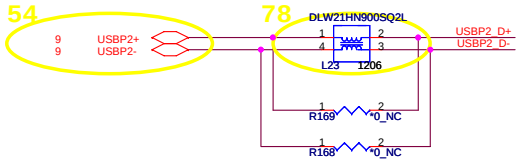
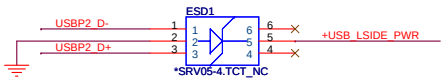
eSATA and USB To DB

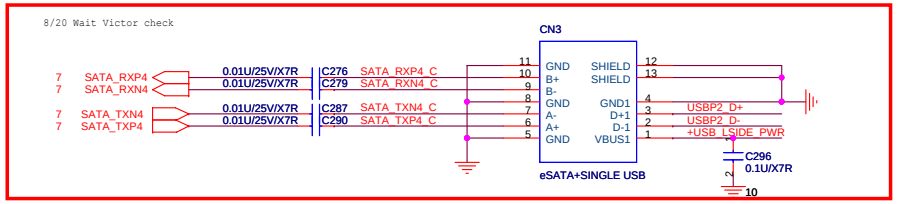
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

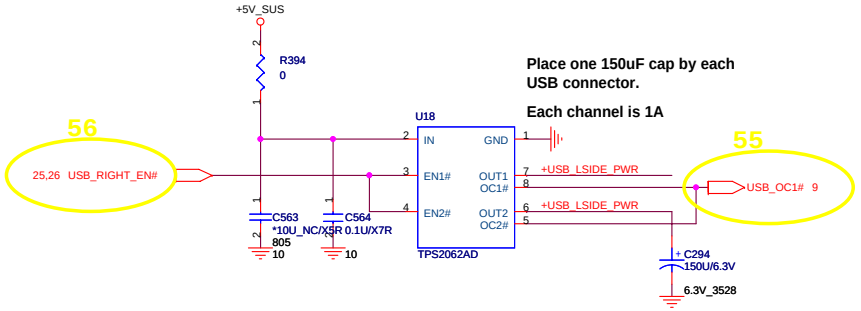


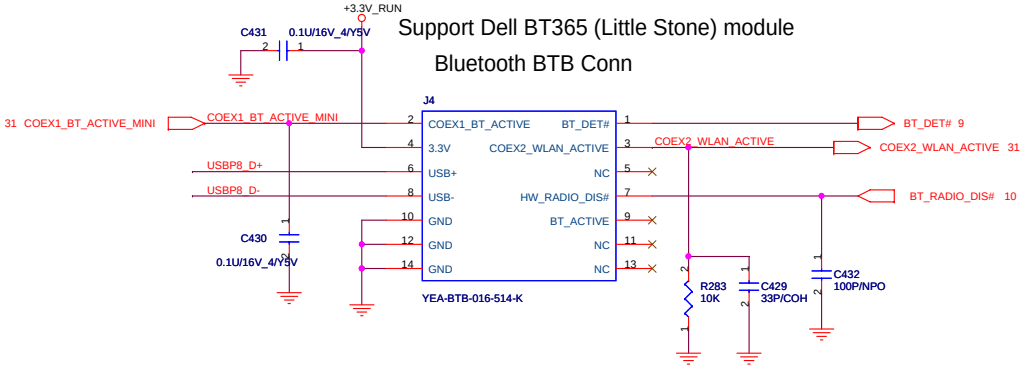
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

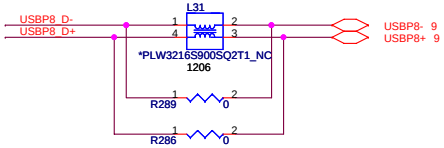


USB and eSATA Conn.









Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	eSATA & Right USB & BT	1A

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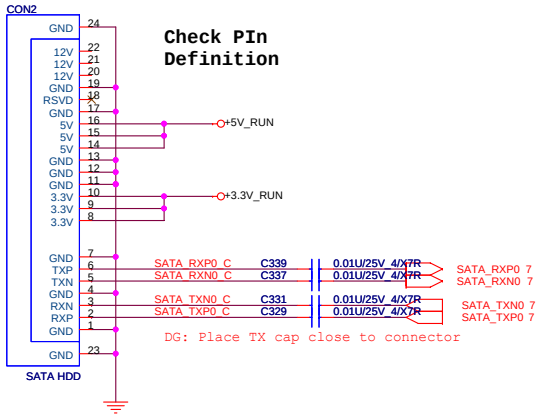
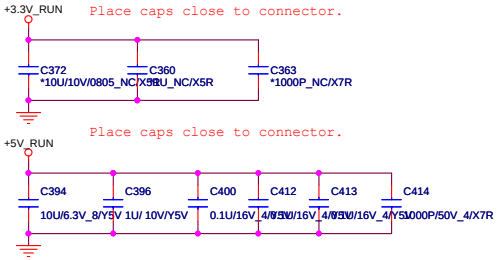
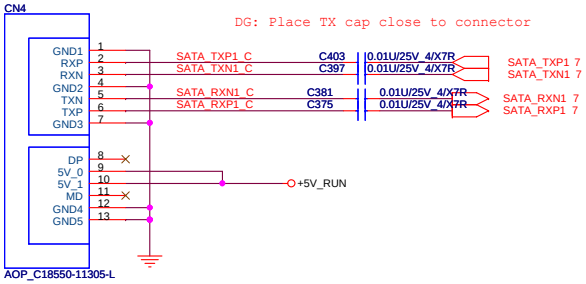
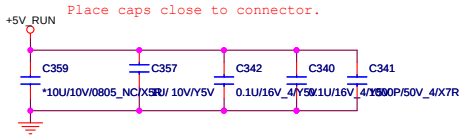
SATA Connector.



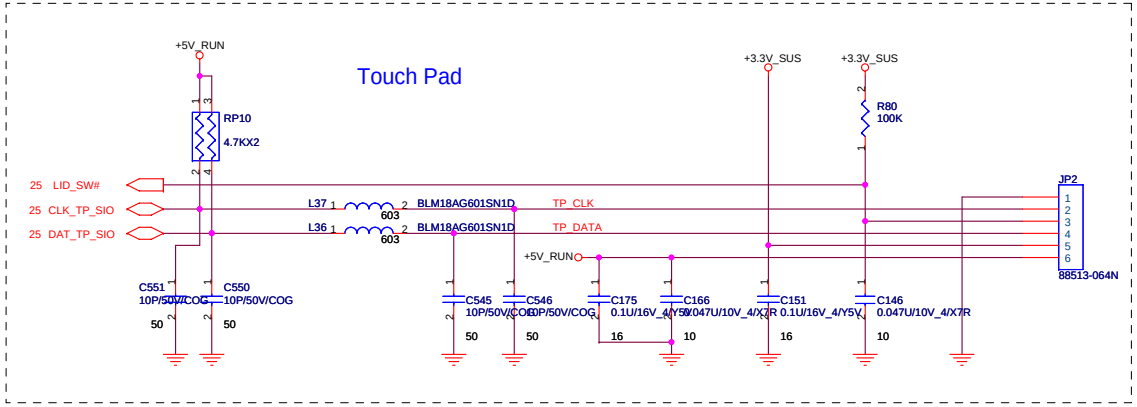


ODD Connector



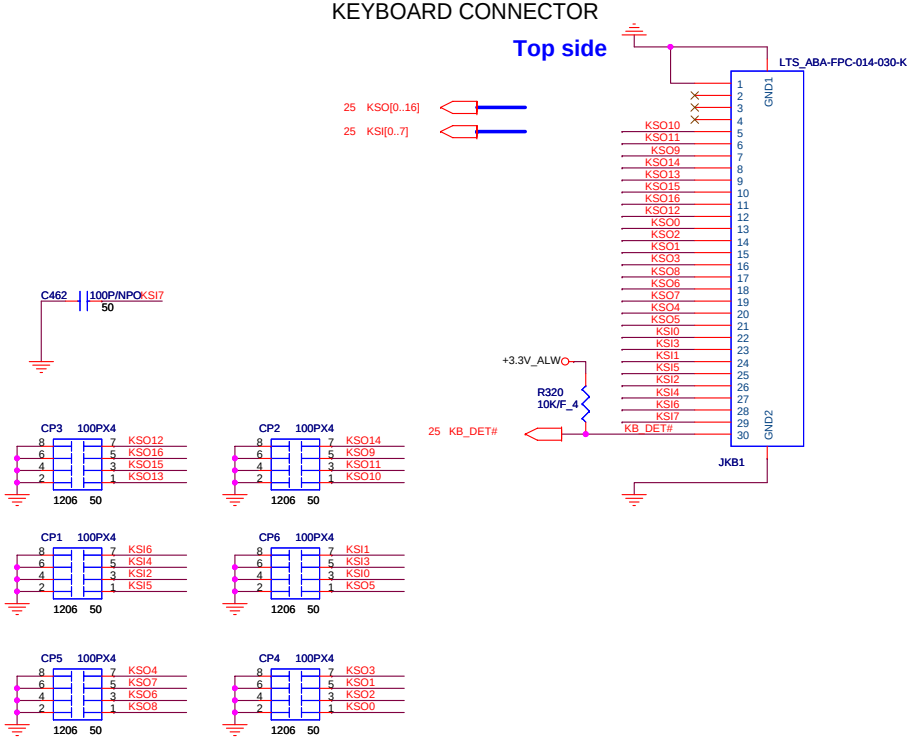


Touch Pad



KEYBOARD CONNECTOR

Top side



100P CAPS CLOSE TO JKB1

Quanta Computer Inc.			
PROJECT : UM8B DIS			
Size	Document Number		Rev
	SATA (HDD&ODD) & TP & KB		1A
Date: Wednesday, November 25, 2009	Sheet 28 of 46		

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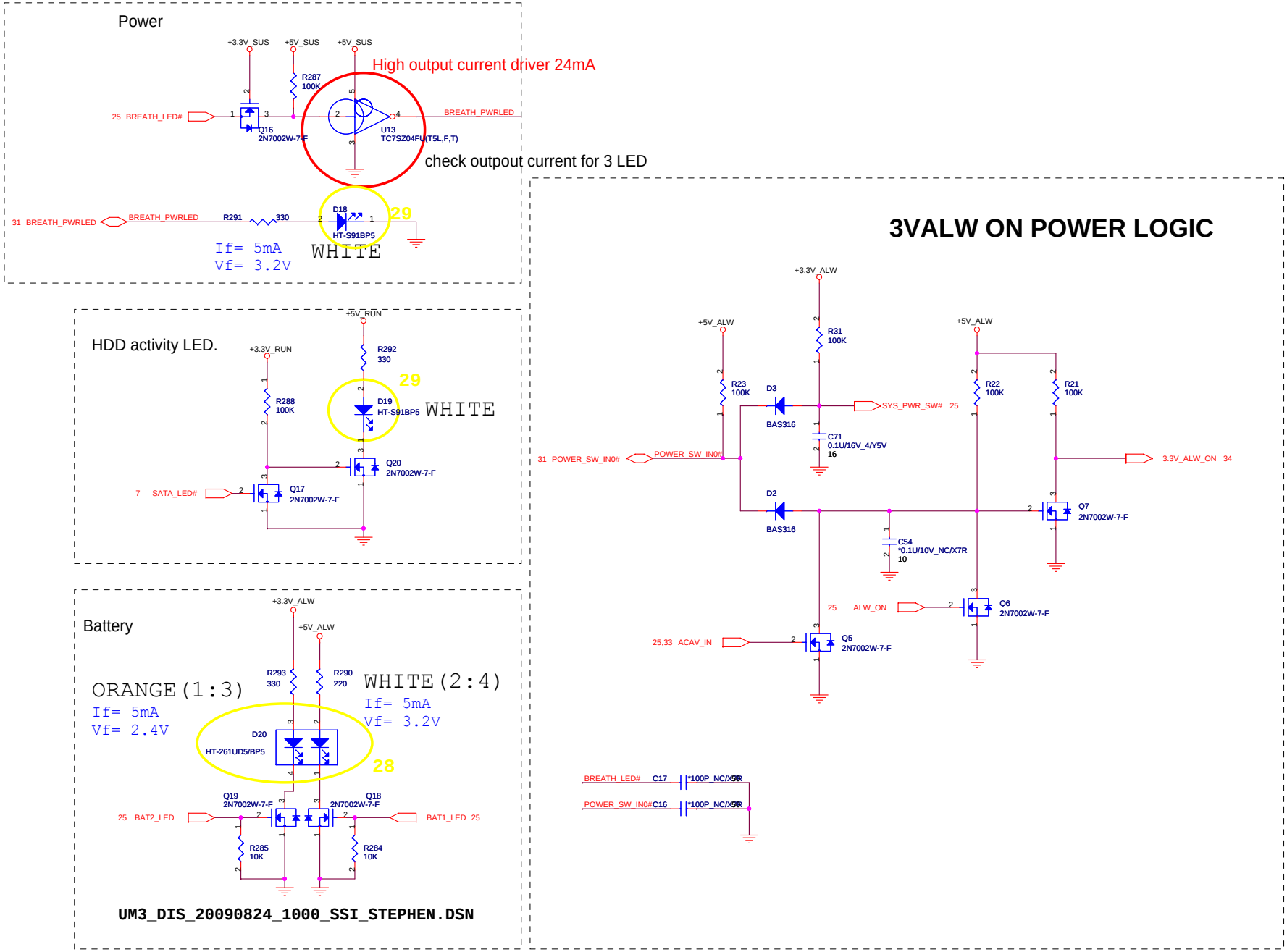

Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	SWITCH, LED	1A

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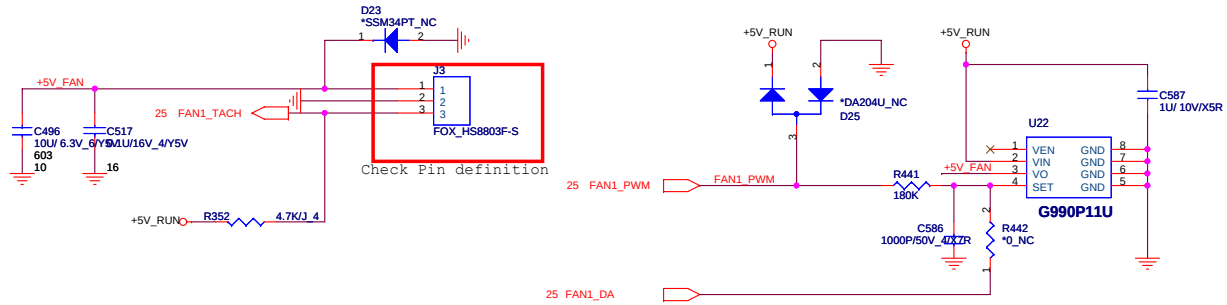
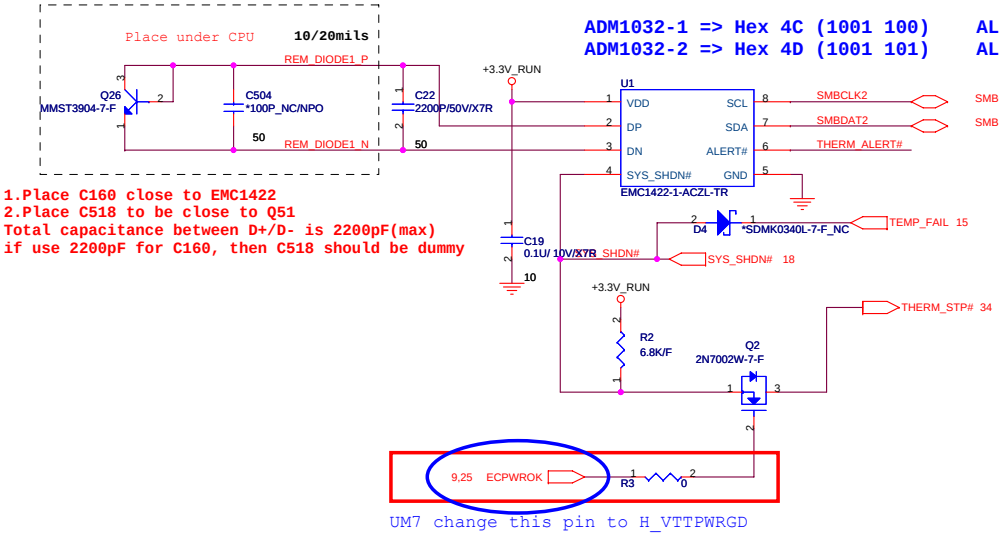
FAN CONTROL

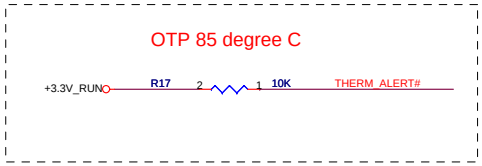




ADM1032-1 => Hex 4C (1001 100) **AL001032001**
ADM1032-2 => Hex 4D (1001 101) **AL001032002**

1.Place C160 close to EMC1422
2.Place C518 to be close to Q51
Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C160, then C518 should be dummy

UM7 change this pin to H_VTTPWRGD



SYS_SHD# / ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	FAN & THERMAL	1A

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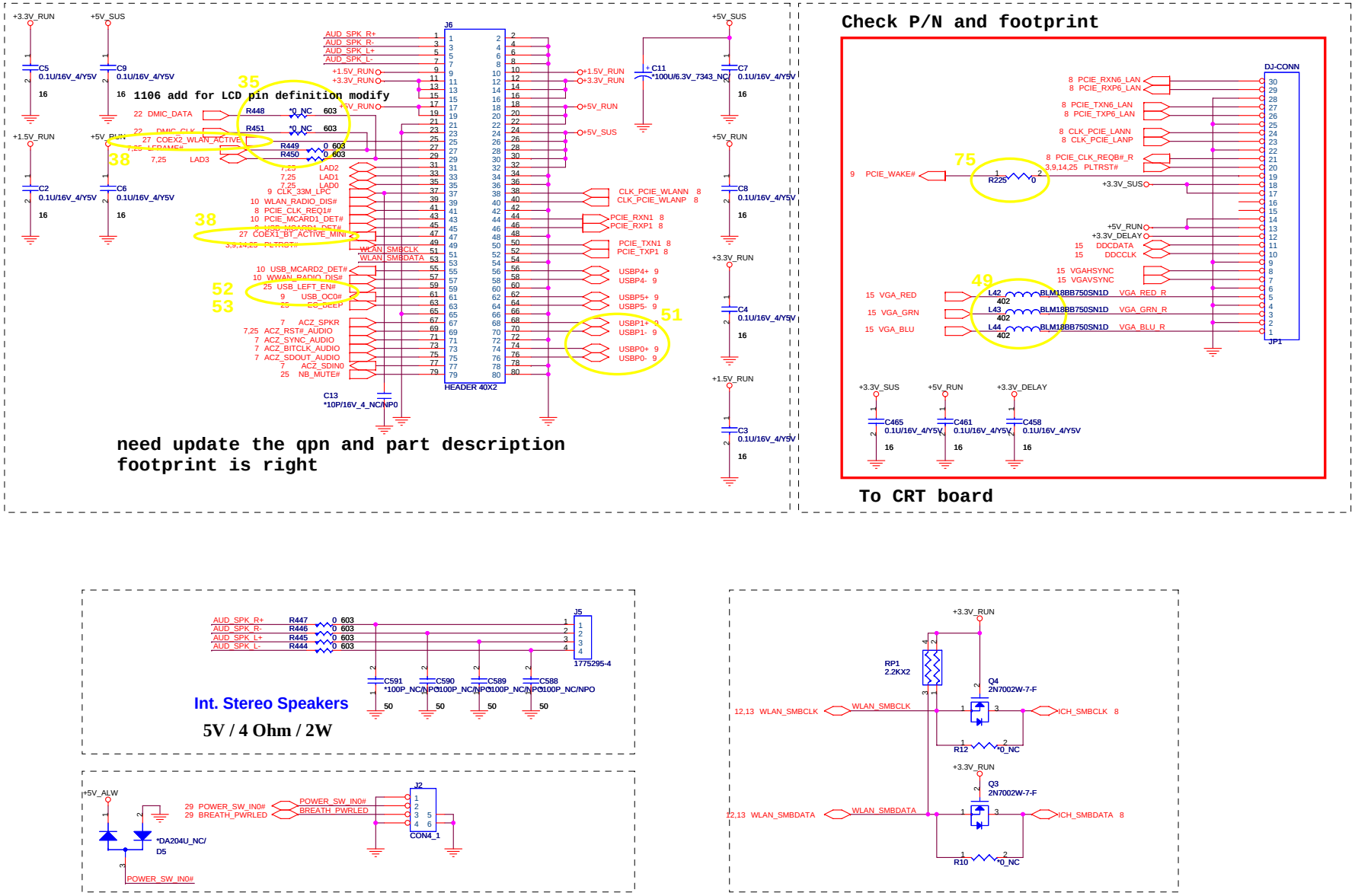

Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	BTB CONN & Audio conn	1A

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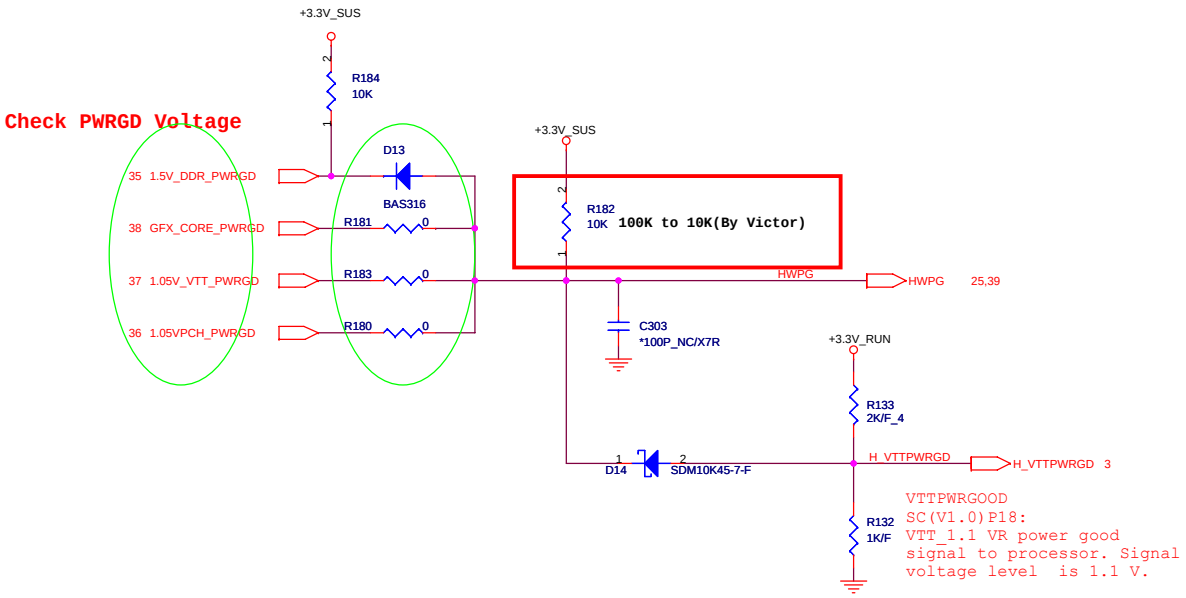

Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	System Reset Circuit	1A

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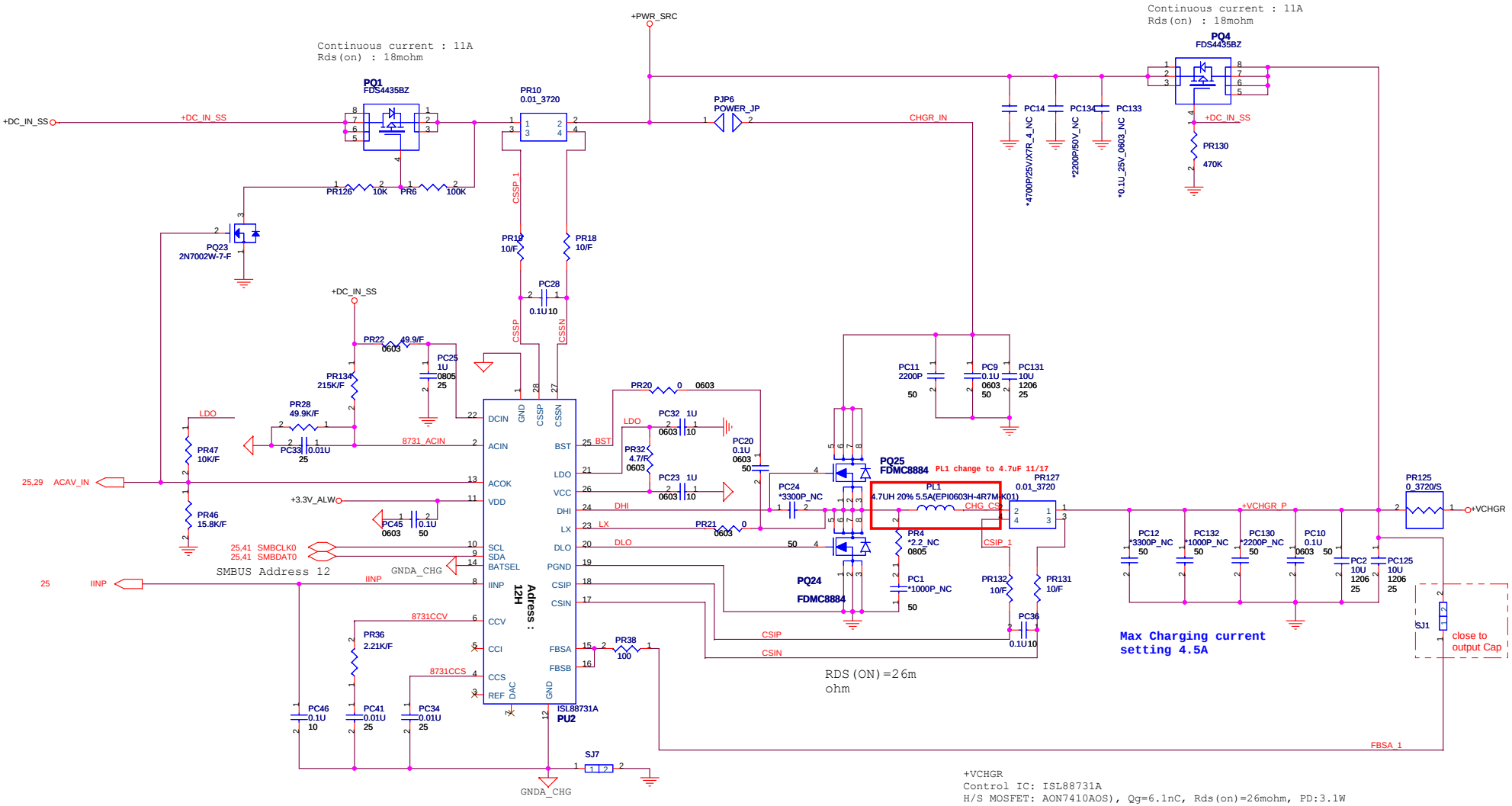

Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	Charger	1A

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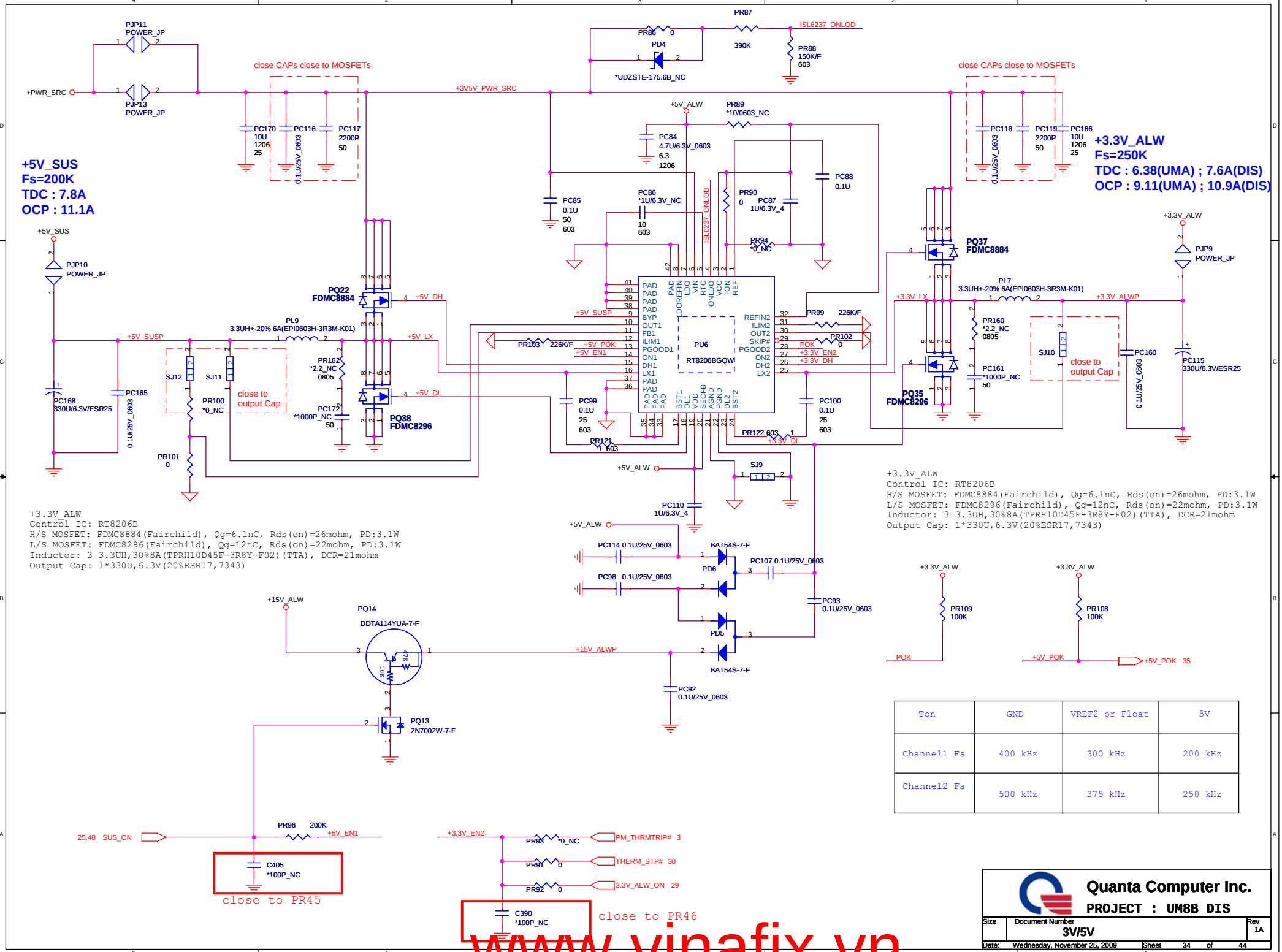

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz

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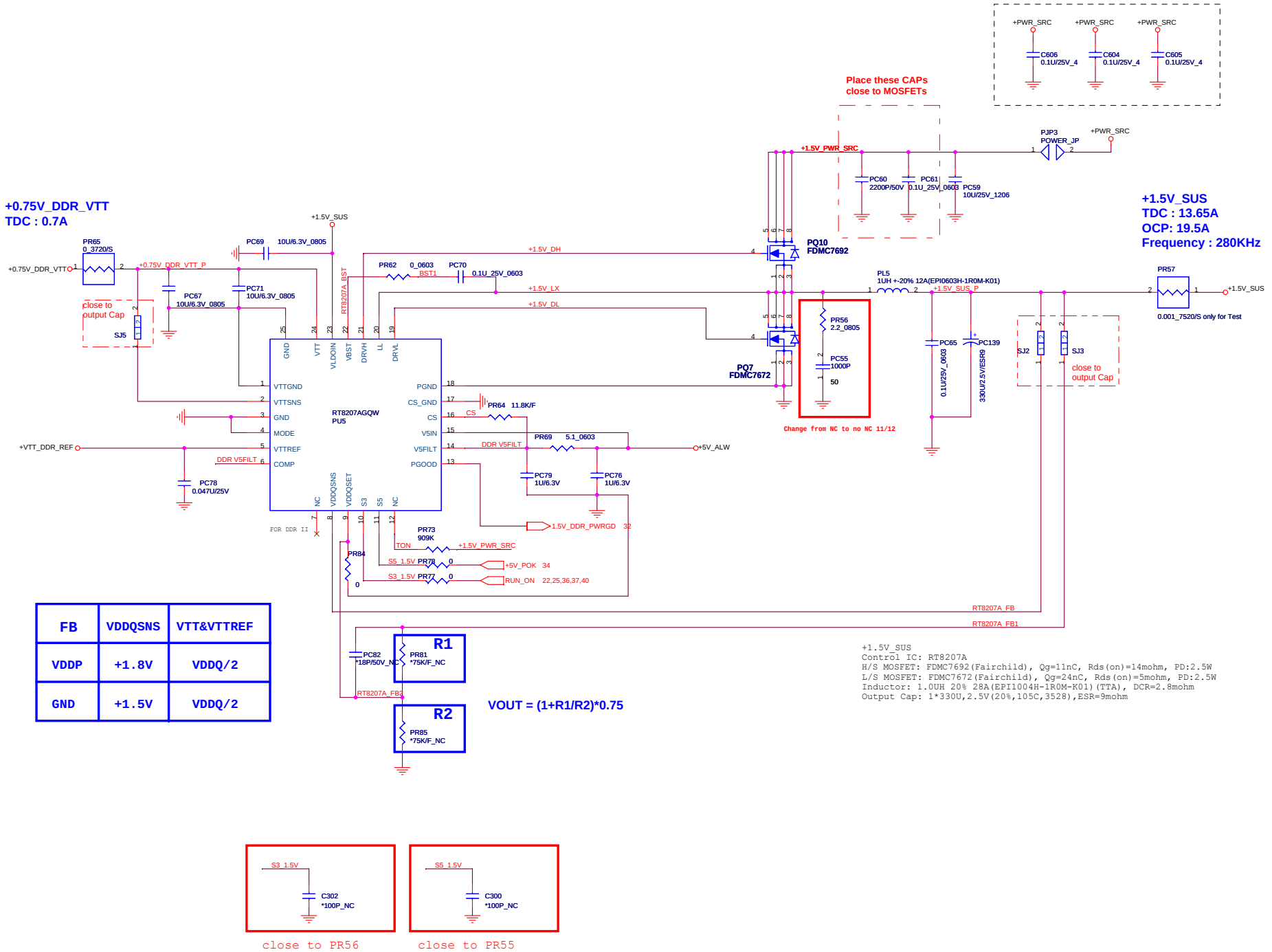

FB	VDDQSNS	VTT&VTTREF
VDDP	+1.8V	VDDQ/2
GND	+1.5V	VDDQ/2

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PROJECT : UM8B DIS

Size	Document Number	Rev
	1.5V_DDR/0.75V	1A

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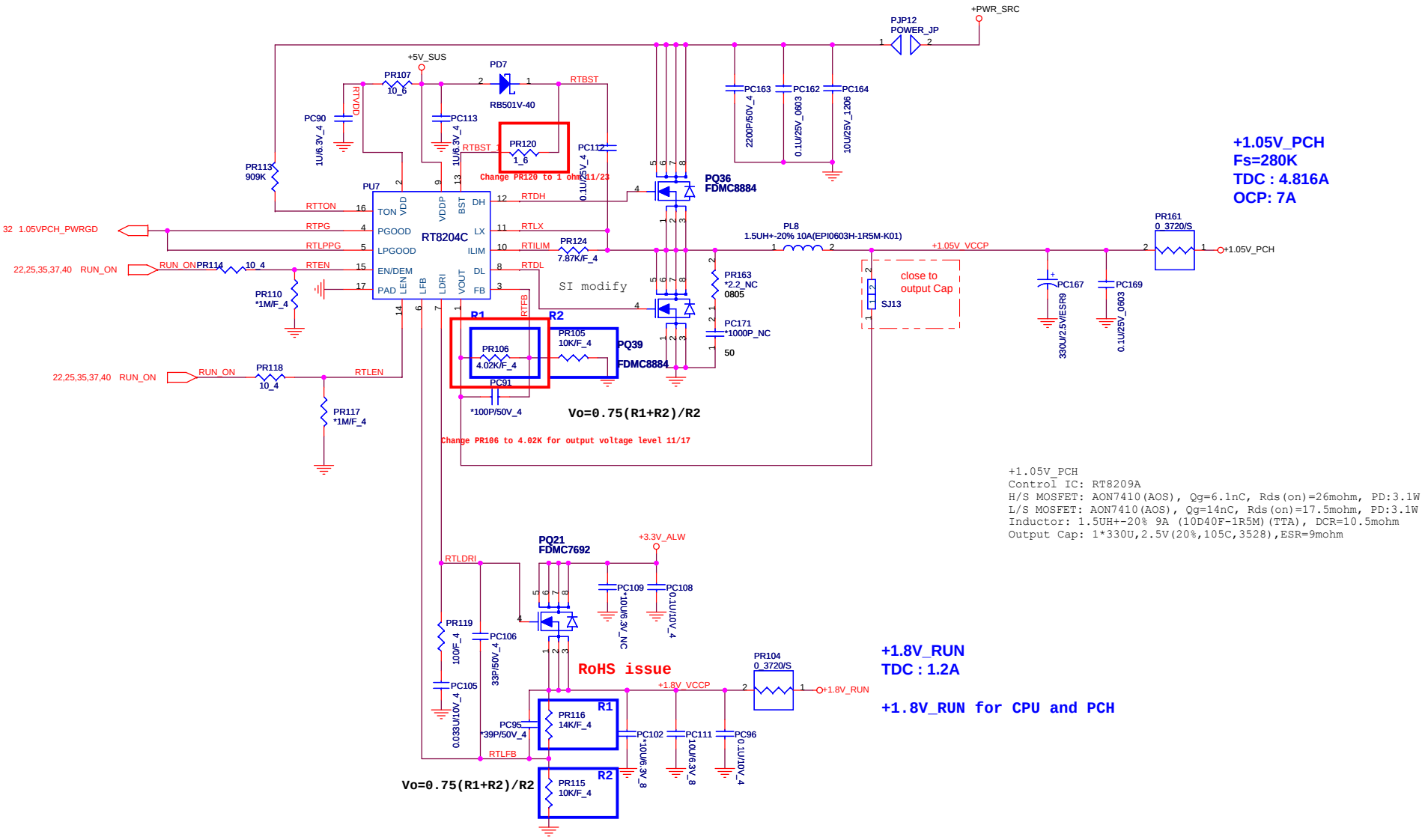

Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	1.05V_PCH	1A

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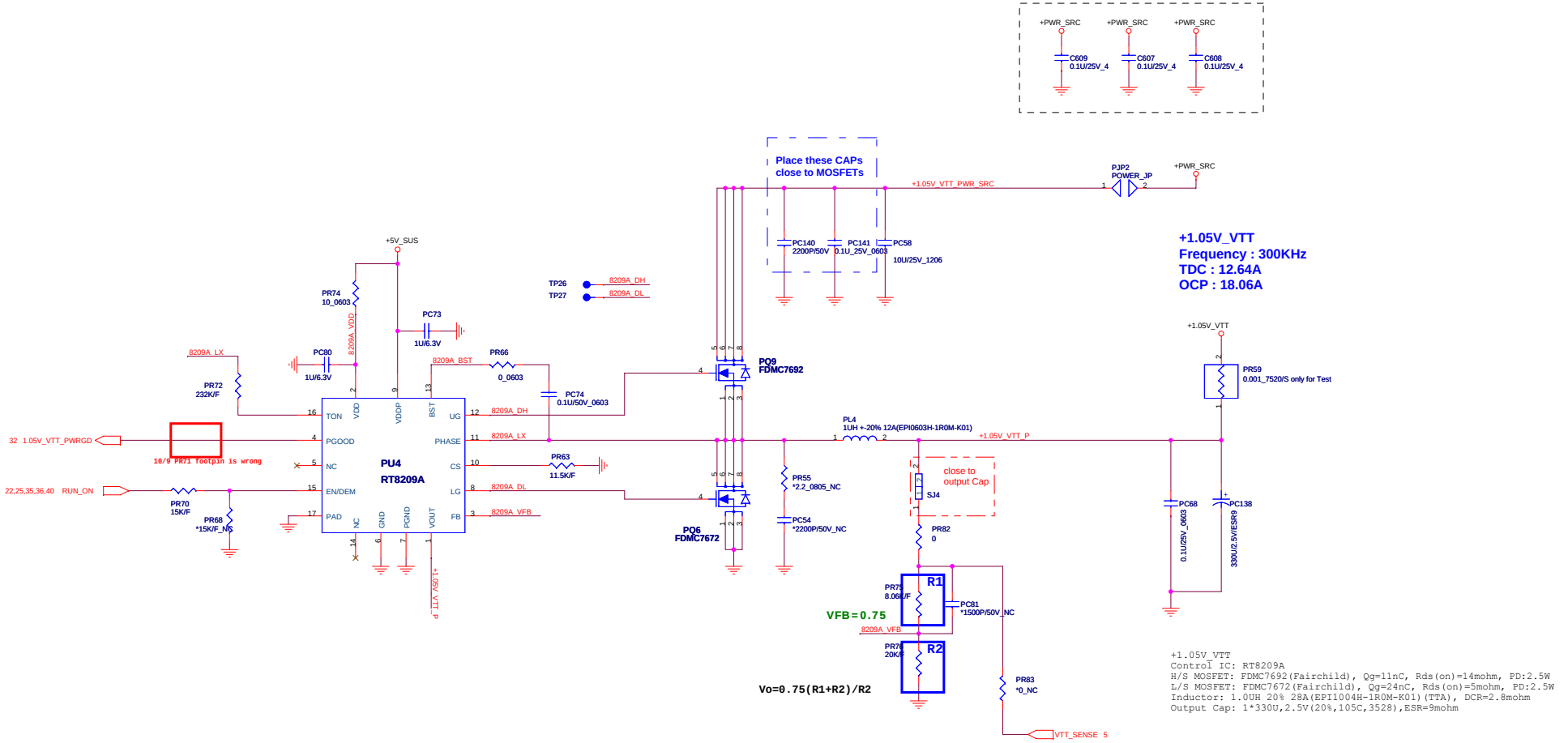

Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	1.05V_VTT	1A

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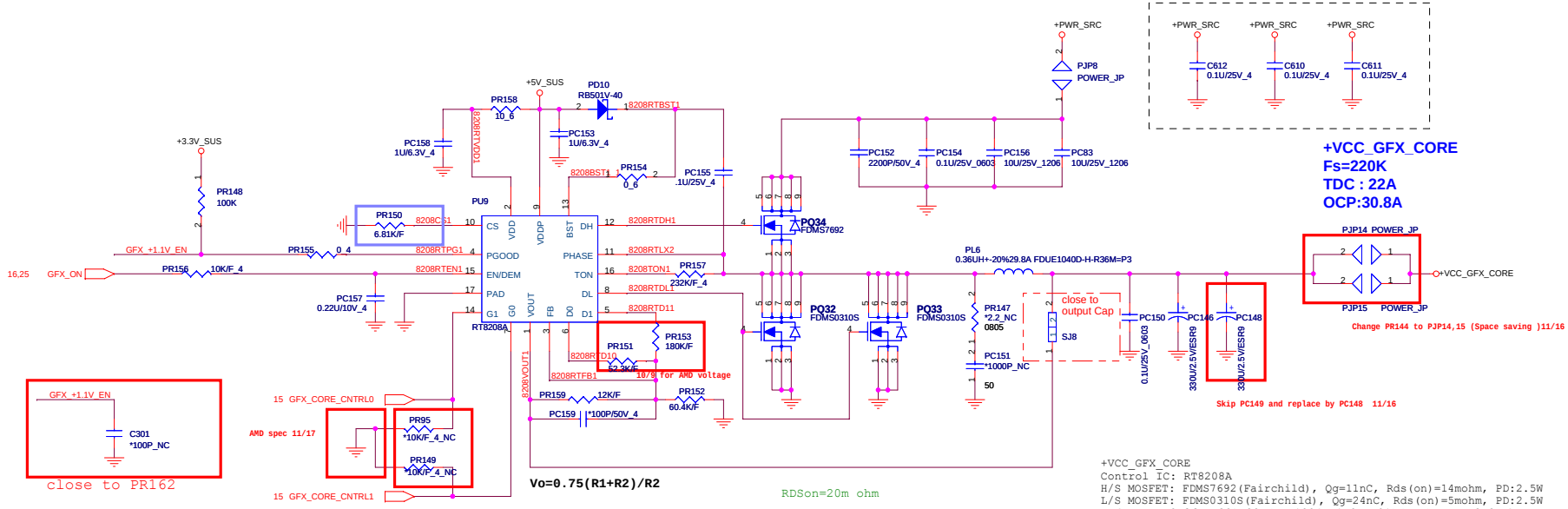
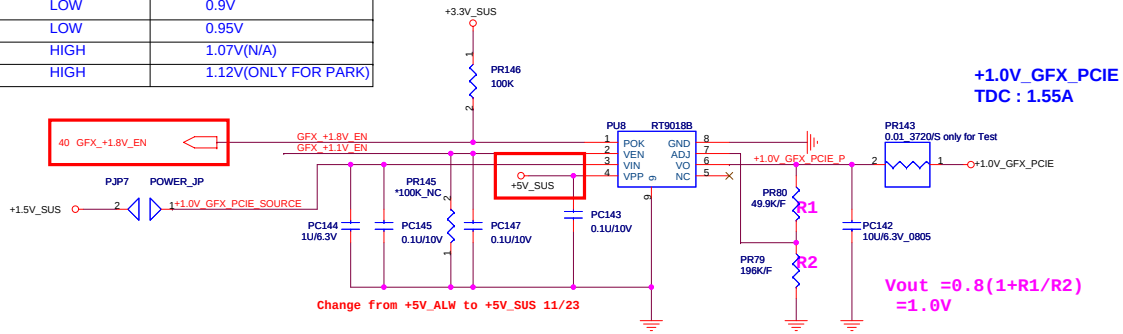
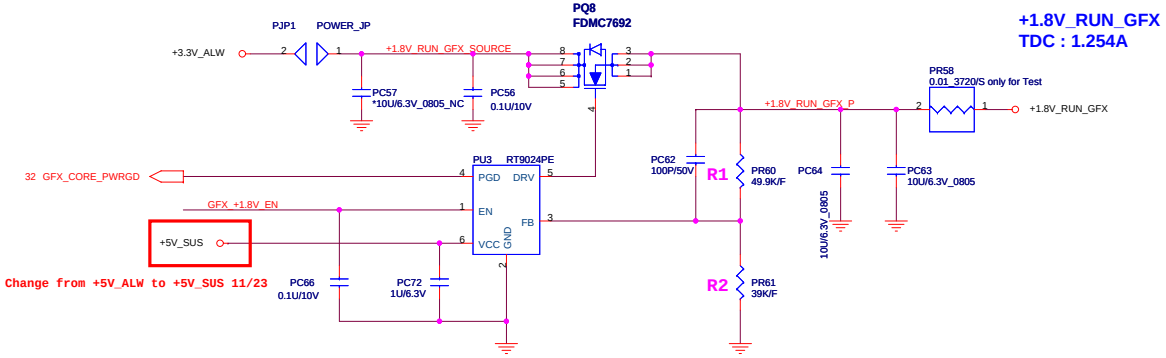


+VCC_GFX_CORE
Control IC: RT8208A
H/S MOSFET: FDMS7692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS0310S(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.36UH 20% 28A(EPI1004H-1R0M-K01)(TTA), DCR=2.8mohm
Output Cap: 2*330U,2.5V(20%,105C,3528),ESR=9mohm

+VCC_GFX_CORE_M92

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
LOW	HIGH	1.07V(N/A)
HIGH	HIGH	1.12V(ONLY FOR PARK)





Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	VGA power	1A

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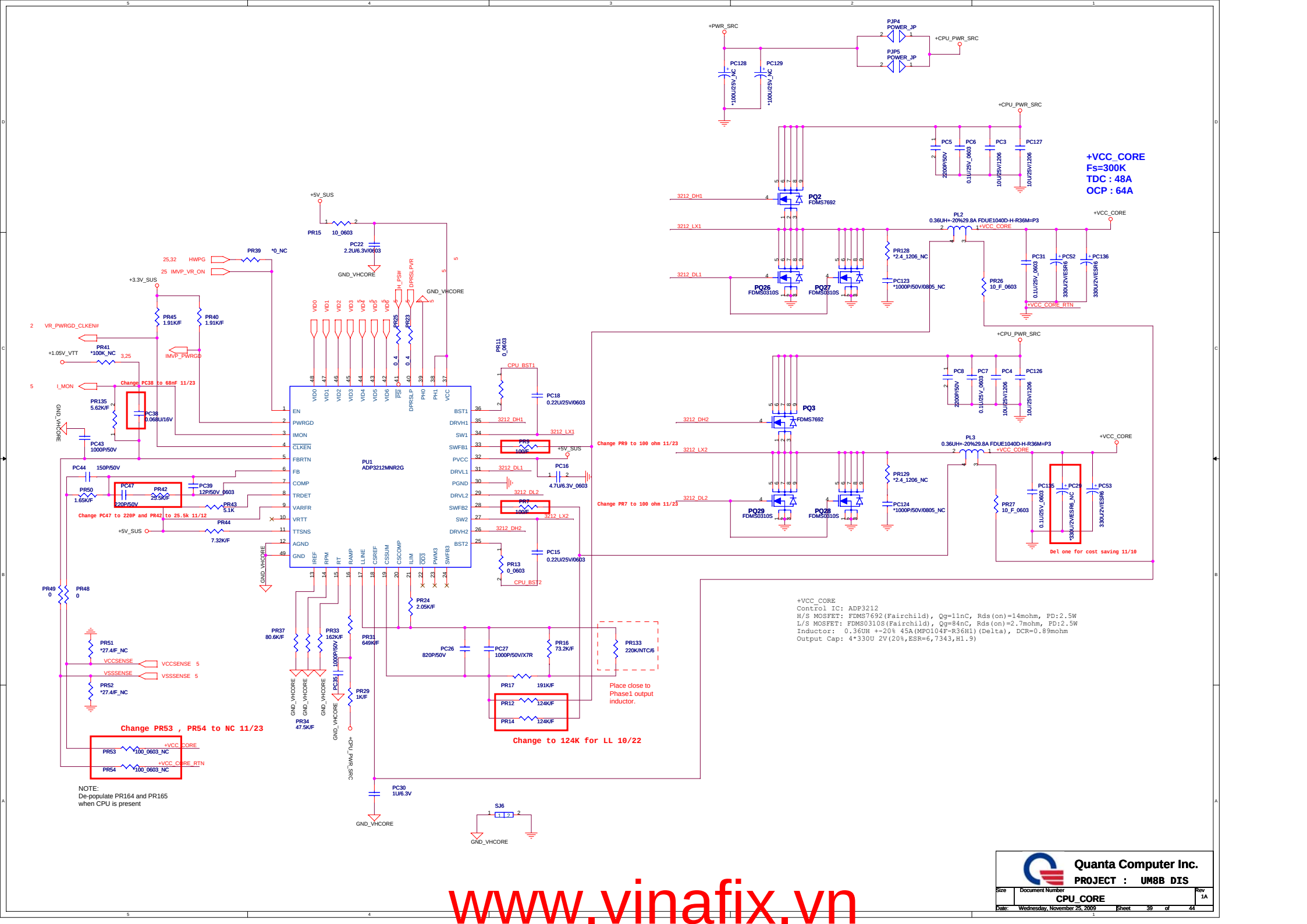
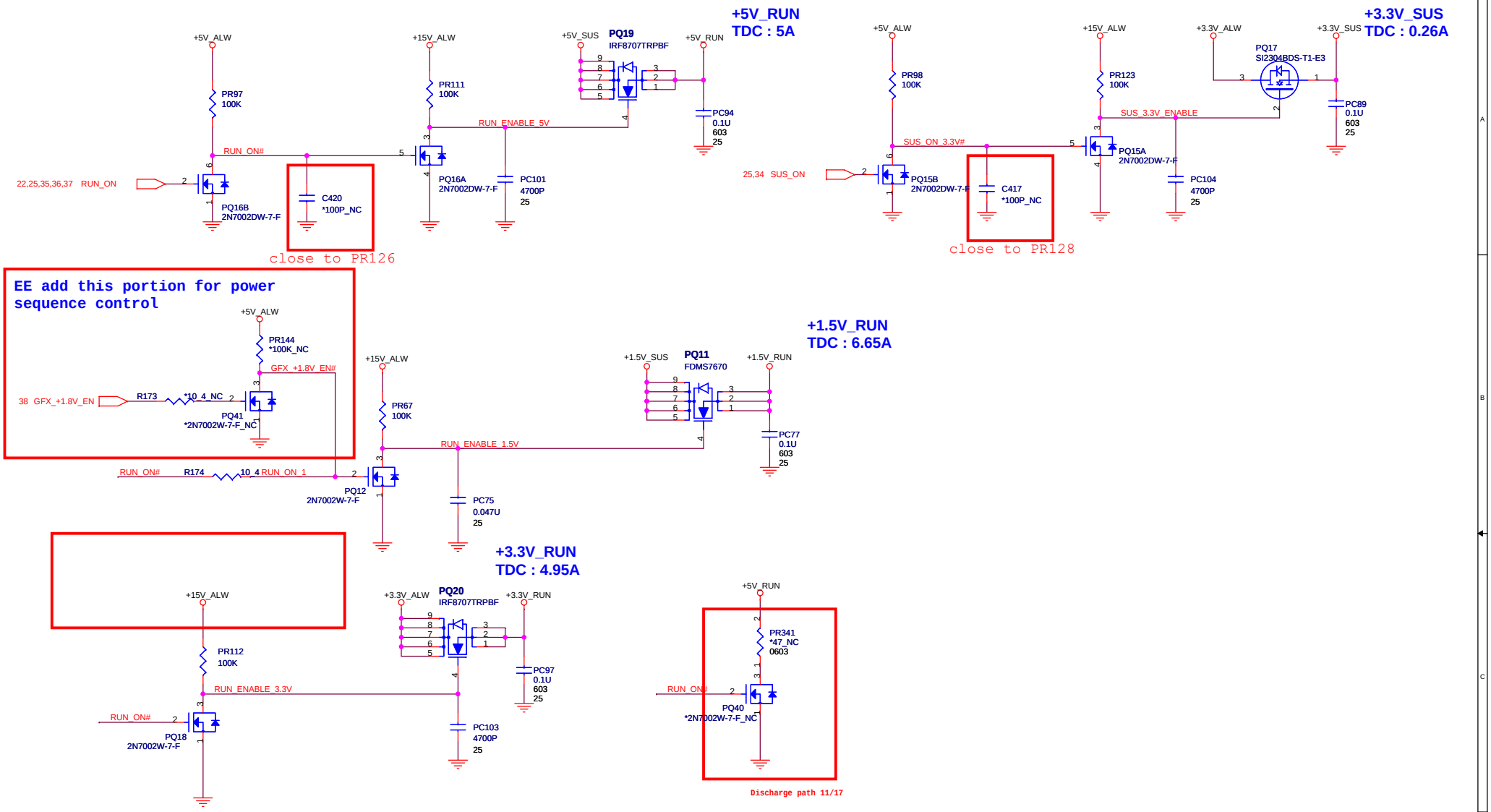


www.vinafix.vn



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PROJECT : UM8B DIS

Size	Document Number	Rev
	Run Power Switch	1A

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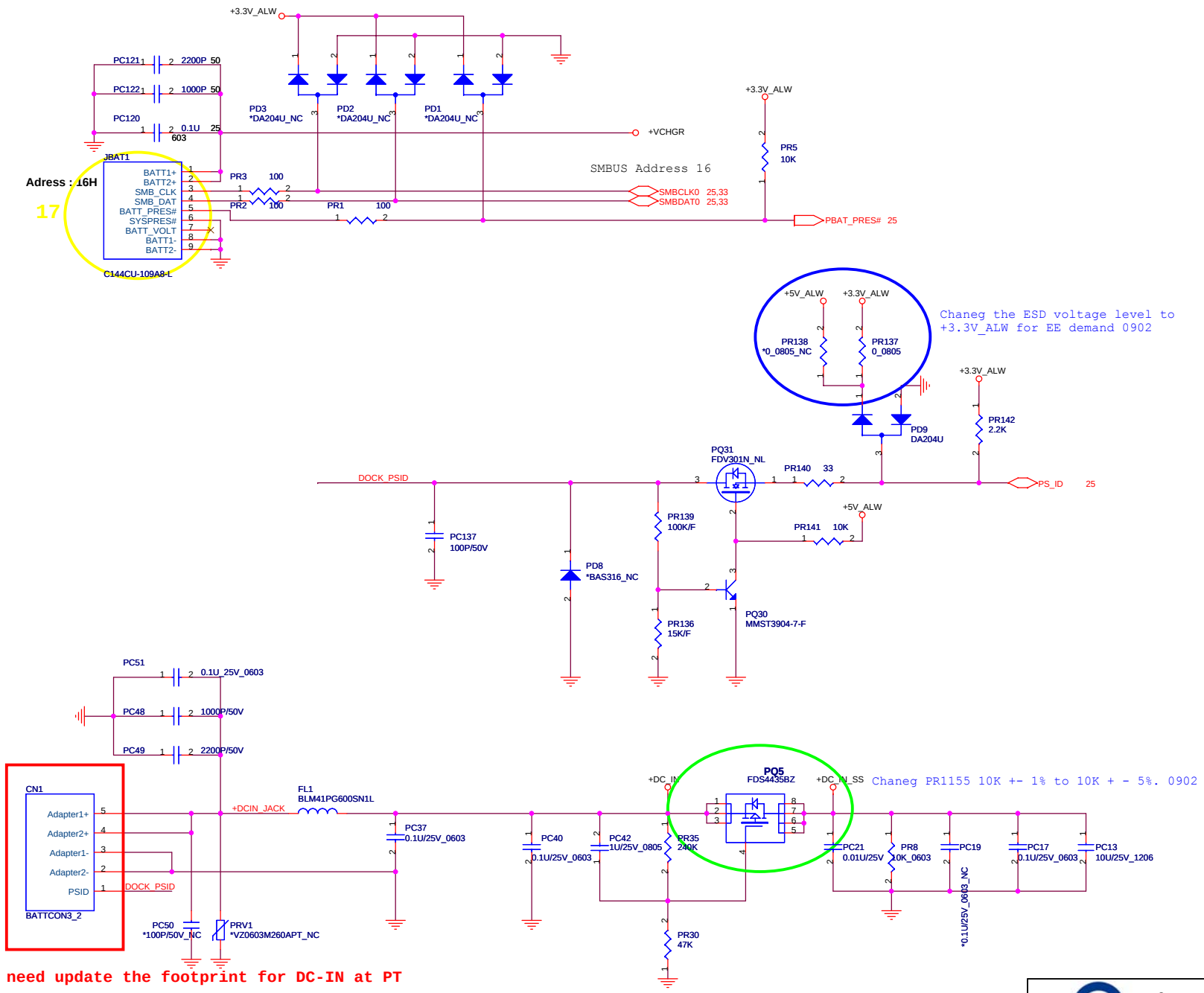

need update the footprint for DC-IN at PT

Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	Batt & DC-IN	1A

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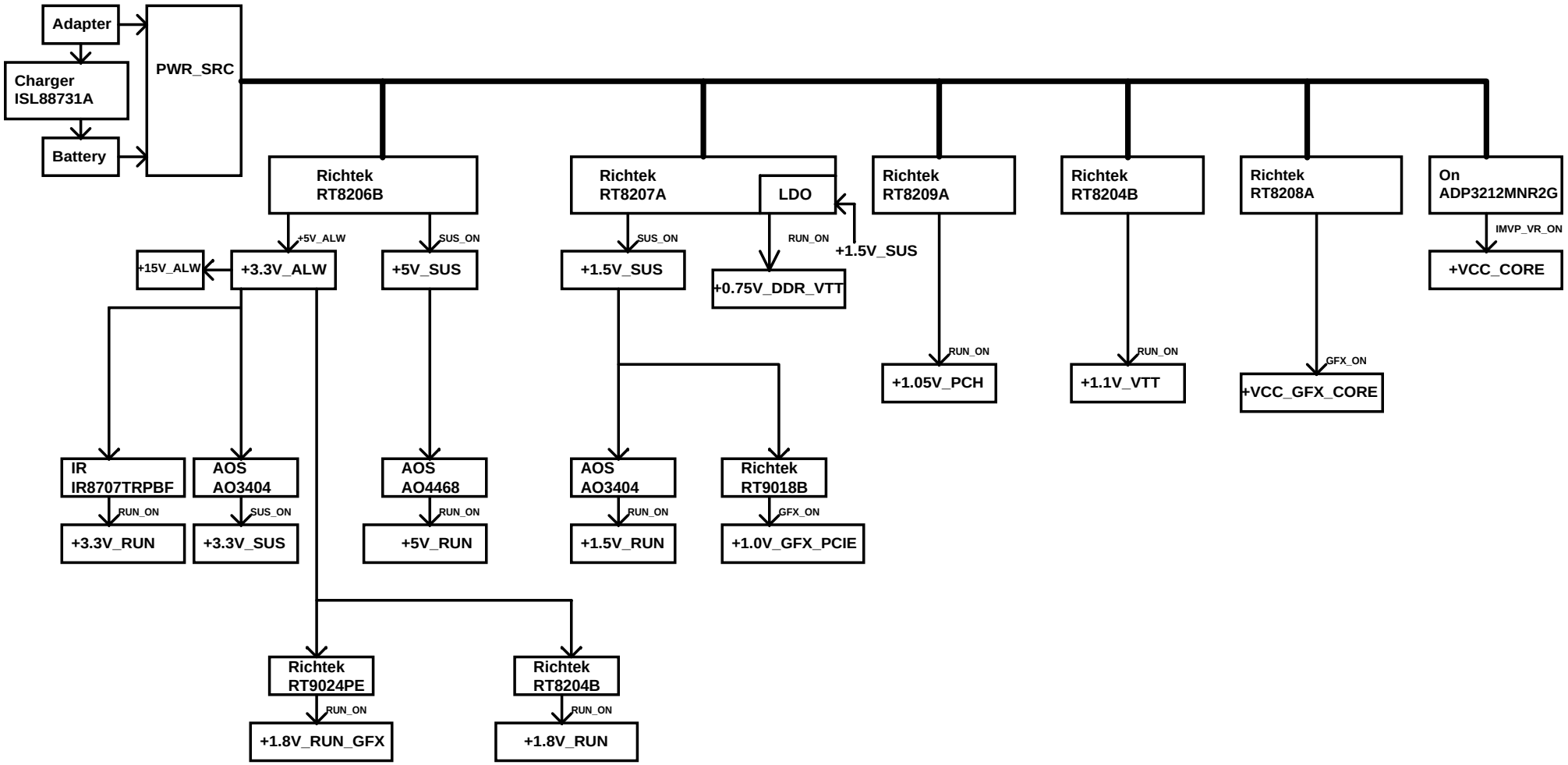
VER : 1A



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PROJECT : UM8B DIS

Size	Document Number	Rev
	Schematic Block Diagram1	1A

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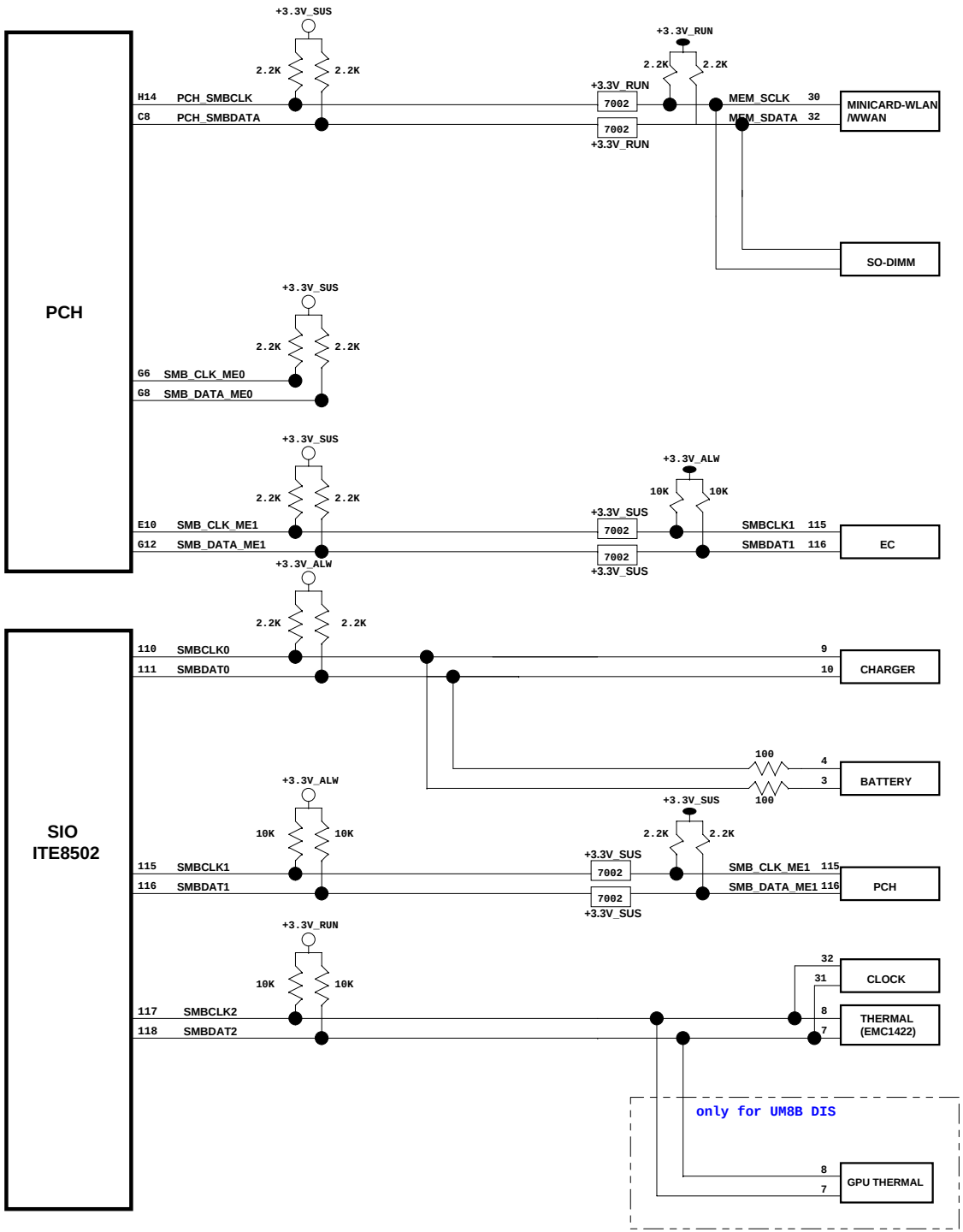

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PROJECT : UM8B DIS

Size	Document Number	Rev
	SMBUS BLOCK	1A

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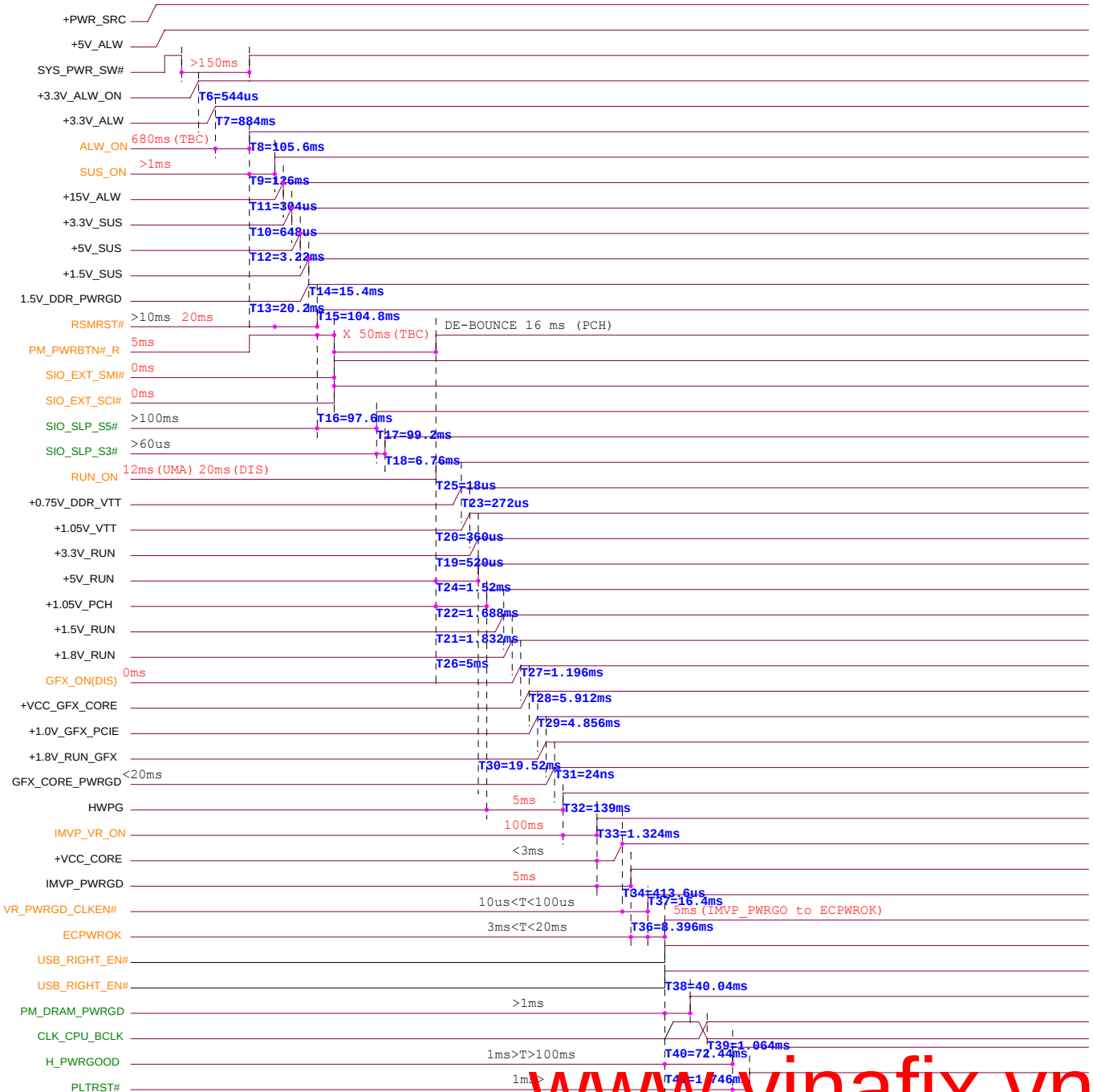
UM8B_ X00 Power On Timing(BATTERY MODE BY SOFTWARE SETUP, W/O ADAPTOR)



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PROJECT : UM8 UMA

Size	Document Number	Rev
	POWER SEQUENCE	1A

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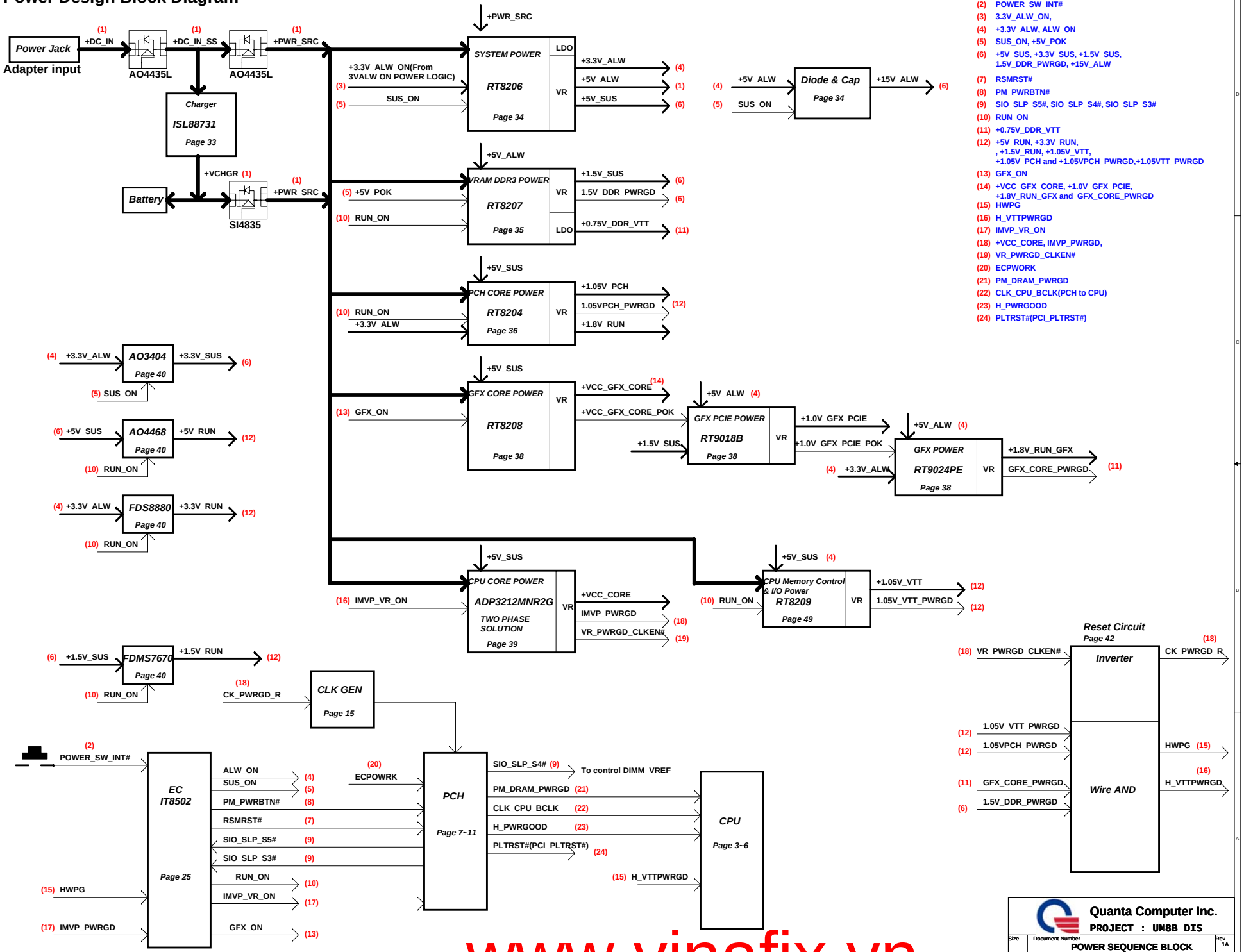
Power Design Block Diagram



(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW
(2) POWER_SW_INT#
(3) 3.3V_ALW_ON,
(4) +3.3V_ALW, ALW_ON
(5) SUS_ON, +5V_POK
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD, +15V_ALW
(7) RSMRST#
(8) PM_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) RUN_ON
(11) +0.75V_DDR_VTT
(12) +5V_RUN, +3.3V_RUN, , +1.5V_RUN, +1.05V_VTT, +1.05V_PCH and +1.05VPCH_PWRGD,+1.05VTT_PWRGD
(13) GFX_ON
(14) +VCC_GFX_CORE, +1.0V_GFX_PCIE, +1.8V_RUN_GFX and GFX_CORE_PWRGD
(15) HWPG
(16) H_VTTPWRGD
(17) IMVP_VR_ON
(18) +VCC_CORE, IMVP_PWRGD,
(19) VR_PWRGD_CLKEN#
(20) ECPWORK
(21) PM_DRAM_PWRGD
(22) CLK_CPU_BCLK(PCH to CPU)
(23) H_PWRGOOD
(24) PLTRST#(PCI_PLTRST#)

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PROJECT : UM8B DIS

Size	Document Number	Rev
	POWER SEQUENCE BLOCK	1A

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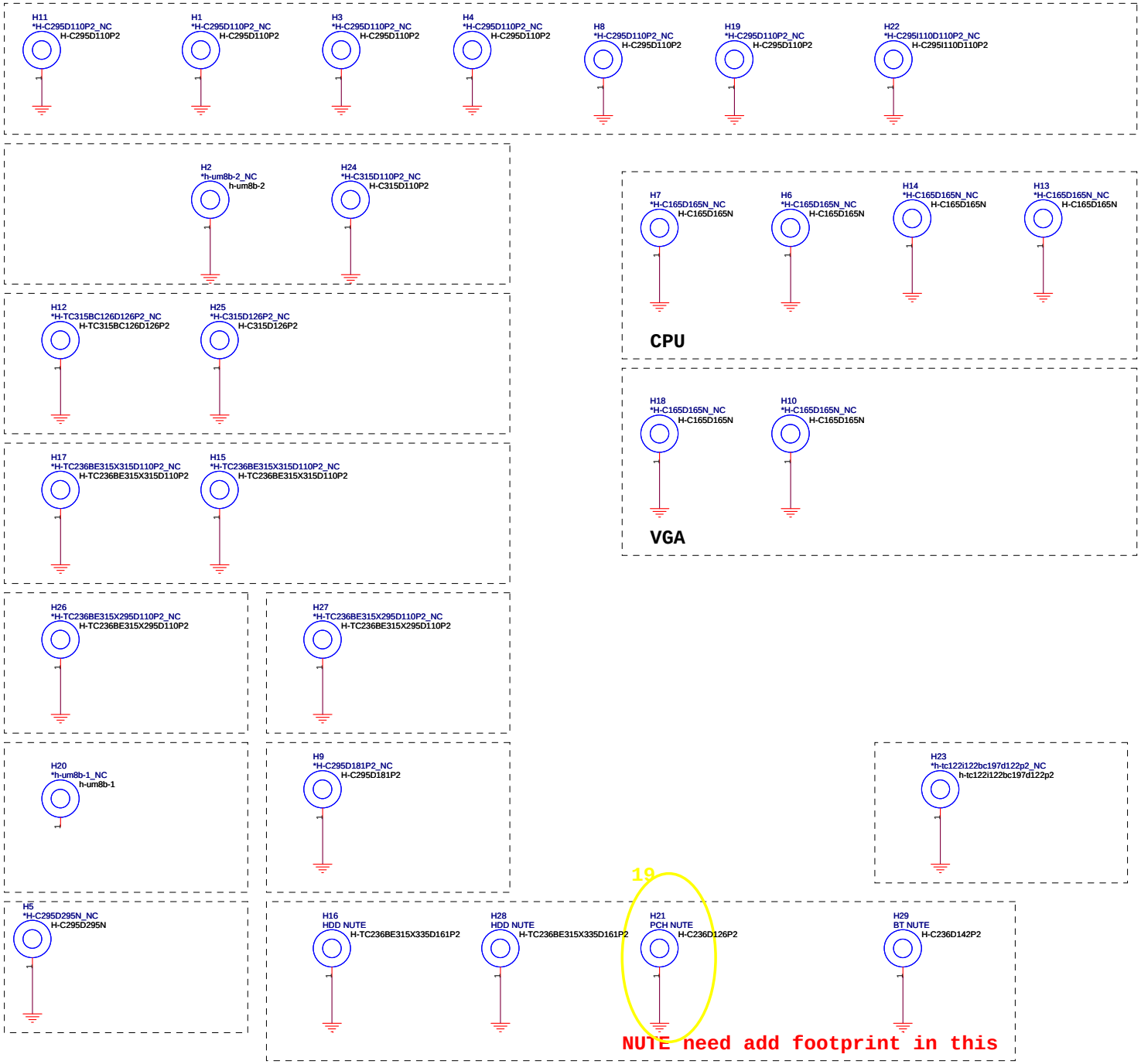

Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	PAD&SCREW	1A

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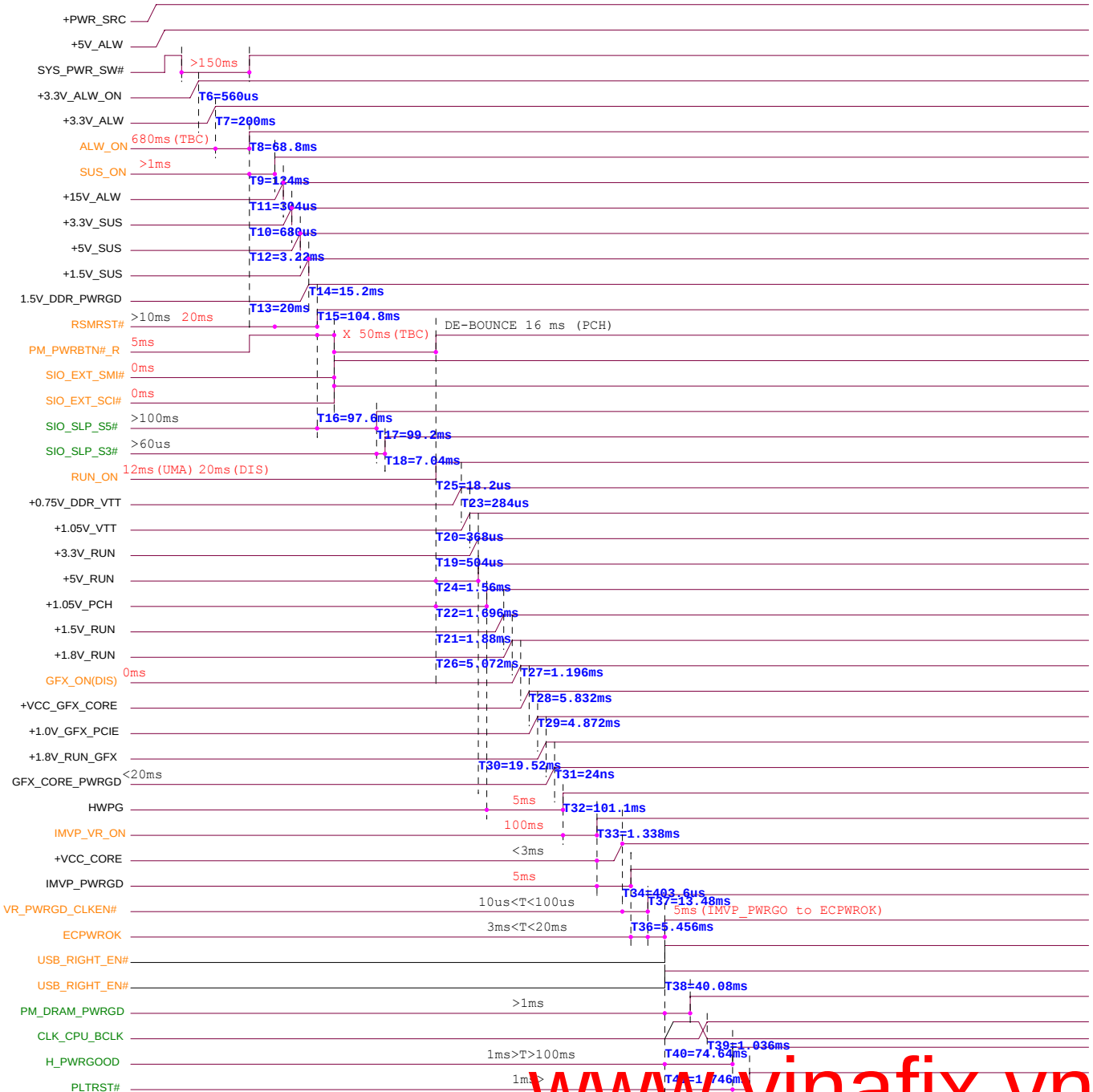
UM8B_ X00 Power On Timing(BATTERY MODE BY SOFTWARE SETUP, W/O ADAPTOR)



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PROJECT : UM8 UMA

Size	Document Number	Rev
	POWER SEQUENCE	1A

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